EE16B
Designing Information Devices and Systems II

Lecture 2B
Transistors I
Announcements

• Last time:
  • Inductance, inductors, transformers
  • Solving diff. EQ for arbitrary inputs
• Today:
  • Lab 2
  • Transistors
ADCs and DACs
R-2R DAC

\[ V_{\text{out}} = V_{\text{max}} \cdot \frac{9}{16} \]

\[
\begin{array}{cccc}
1 & 0 & 0 & 1 \\
2^3 & 2^2 & 2^1 & 2^0
\end{array}
\]
R-2R DAC

Solve Via Super Position!
R-2R DAC
R-2R DAC

\[ V_{out} = \frac{V_{bN}}{2} \]
R-2R DAC

\[ V_{out} = \frac{V_{b0}}{2^N} + \frac{V_{b1}}{2^{N-1}} + \ldots + \frac{V_{bN}}{2} \]
R-2R DAC

\[ V_{\text{out}} \]

\[ V_{\text{ref}} \cdot \frac{9}{16} \]

\[ \begin{align*}
    &1 &0 &0 &1 \\
    \rightarrow &9/16
\end{align*} \]

\[ \begin{align*}
    2^3 &2^2 &2^1 &2^0
\end{align*} \]
Lab 2: SAR ADC

- Successive Approximation Resistor
- Use DAC to guess bit by bit
- Iterate \((\log(N))\) times
Devices as part of a system

- Resistor
- Capacitor
- Inductor
- Diode
- Transistor
Transistor

First transistor - Dec 1947

First integrated circuit 1958
Computational advances due to fabrication advances

Moore's law is the observation that the number of transistors in a dense integrated circuit doubles approximately every two years.
FinFET—A Self-Aligned Double-Gate MOSFET
Scalable to 20 nm

Dighi Hlsamoto, Member, IEEE, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, Member, IEEE, Charles King, Erik Andersen, Tsu-Jae King, Jeffrey Bokor, Fellow, IEEE, and Chenming Hu, Fellow, IEEE

Abstract—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped Si_xGe_1−x as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasi-planar nature of this new variant of the vertical-double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.

Index Terms—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.

I. INTRODUCTION

To develop sub-50 nm MOSFETs, the double-gate structure has been widely studied. This is because

source: Intel

33 nm

53 nm

source: Chinese Academy of Microelectronics

Go Bears!
Sense of Scale

Source: Mark Bohr, IDF14
MOS Transistor

- MOS: metal-oxide-semiconductor
- MOSFET: MOS field effect Transistor
- Two kinds:
  - NMOS - current carried by electrons
  - PMOS - current carried by “holes” (lack of e)
Simplest Circuit Model of NMOS

Or:

\[ V_{GS} \geq V_{t_n} \]

Or:
Simplest Circuit Model of NMOS

\[ V_{GS} < V_{t_n} \]
Simplest Circuit Model for NMOS

\[ V_{GS} < V_{t_n} \]

\[ V_{GS} \geq V_{t_n} \]
Simple NMOS Inverter

![NMOS Inverter Diagram]

- $V_{in}$
- $G$
- $S$
- $D$
- $V_{out}$
- $V_{DD}$

Logic Inverter:
- Low Input → High Output
- High Input → Low Output
Simple NMOS Inverter

Low
High
High
Low

\[ V_{GS} < V_{t_n} \]

\[ V_{GS} \geq V_{t_n} \]

Logic Inverter

Low, High

High, Low
Simplest Circuit Model of PMOS

Or:

\[ V_{GS} \leq -|V_{tp}| \]
CMOS (Complementary MOS)

- PMOS + NMOS
- Very low power consumption inverter
- Dominant technology

![Diagram of CMOS inverter circuit]
CMOS (Complementary MOS)

V_{in} = V_{DD} \Rightarrow "1"

PMOS: V_{GS} = 0 > -|V_{t_{p}}|
\Rightarrow \text{Off, open circuit}

NMOS: V_{GS} = V_{DD} > V_{t_{n}}
\Rightarrow \text{On, short circuit}
CMOS (Complementary MOS)

- **NMOS**: $V_{GS} = V_{DD} > V_{t_n}$
  - $V_{in} = V_{DD} \Rightarrow "1"
  - $V_{out} = 0V \Rightarrow "0"
  - Off, open circuit
  - On, short circuit

- **PMOS**: $V_{GS} = 0 > -|V_{t_p}|$
  - Off, open circuit
CMOS (Complementary MOS)

\[ V_{in} = 0 \quad \Rightarrow \quad \text{"0"} \]

PMOS: \[ V_{GS} = -V_{DD} < -|V_{t_p}| \]
\[ \Rightarrow \text{On, short circuit} \]

NMOS: \[ V_{GS} = 0 < V_{t_n} \]
\[ \Rightarrow \text{Off, open circuit} \]
CMOS (Complementary MOS)

\[ V_{\text{in}} = 0 \Rightarrow "0" \]

PMOS: \( V_{\text{GS}} = -V_{\text{DD}} < -|V_{t_p}| \)
\( \Rightarrow \) On, short circuit

\( \overline{\text{NMOS}}: V_{\text{GS}} = 0 < V_{t_n} \)
\( \Rightarrow \) Off, open circuit

\[ V_{\text{out}} = V_{\text{DD}} \Rightarrow "1" \]
CMOS (Complementary MOS)

Simplest Circuit Model for NMOS

\[ \text{Diagram of NMOS device with control points } V_{\text{in}}, V_{\text{out}}, V_{\text{DD}} \]

\[ \text{Graph showing } V_{\text{out}} \text{ vs. } V_{\text{in}} \]
CMOS (Complementary MOS)

Simplest Circuit Model for NMOS

\( V_{in} \)  \( V_{out} \)  \( V_{DD} \)
CMOS (Complementary MOS)

Simplest Circuit Model for NMOS

\( V_{in} \) to \( V_{out} \)

- NMOS OFF
- NMOS On
- PMOS OFF
- PMOS On
CMOS (Complementary MOS)

Simplest Circuit Model for NMOS

\[ V_{in} \rightarrow V_{out} \]

\[ V_{DD} \]

\[ V_{in} \rightarrow V_{out} \]

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\[ V_{in} \rightarrow V_{out} \]

\[ V_{DD} \]
CMOS (Complementary MOS)

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<th>$V_A$</th>
<th>$V_B$</th>
<th>$M_1$</th>
<th>$M_2$</th>
<th>$M_3$</th>
<th>$M_4$</th>
<th>$V_{out}$</th>
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<td>On</td>
<td>Off</td>
<td>Off</td>
<td>$V_{DD}$</td>
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<tr>
<td>0</td>
<td>1</td>
<td>On</td>
<td>Off</td>
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<tr>
<td>1</td>
<td>1</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
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NAND gate!