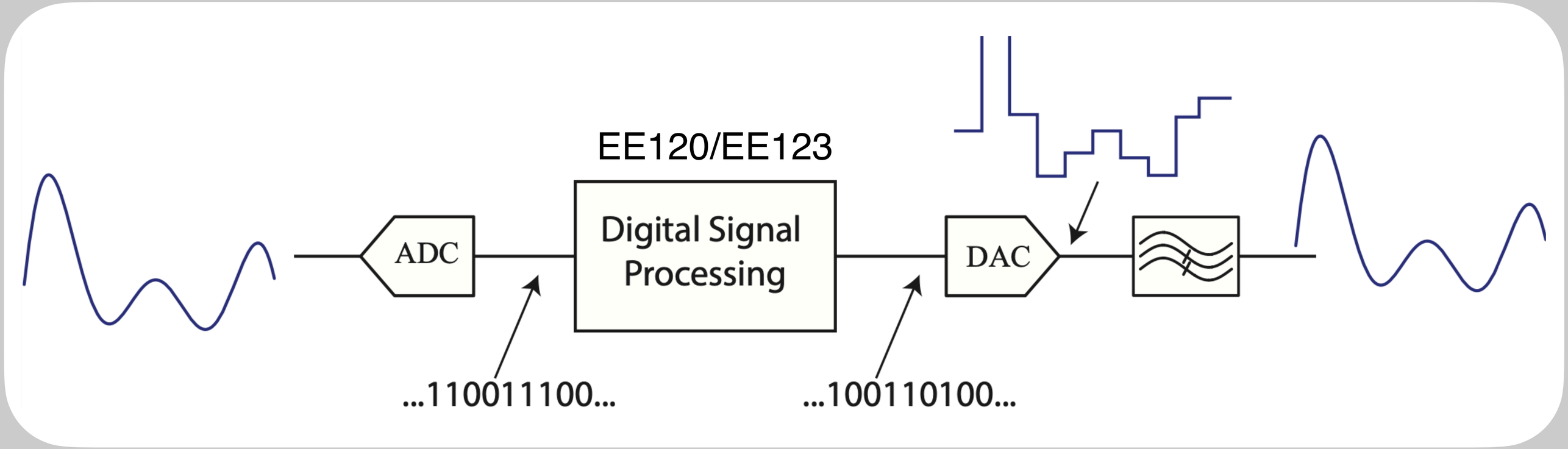
EE16B
Designing Information Devices and Systems II

Lecture 2B
Transistors I

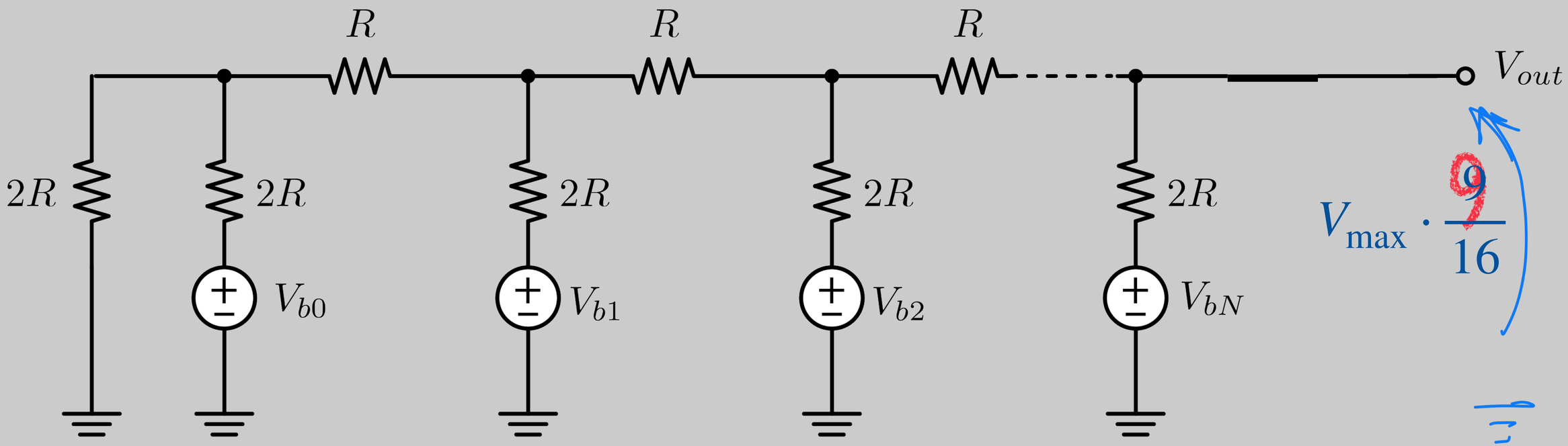
Announcements

- Last time:
  - Inductance, inductors, transformers
  - Solving diff. EQ for arbitrary inputs
- Today:
  - Lab 2
  - Transistors

ADCs and DACs



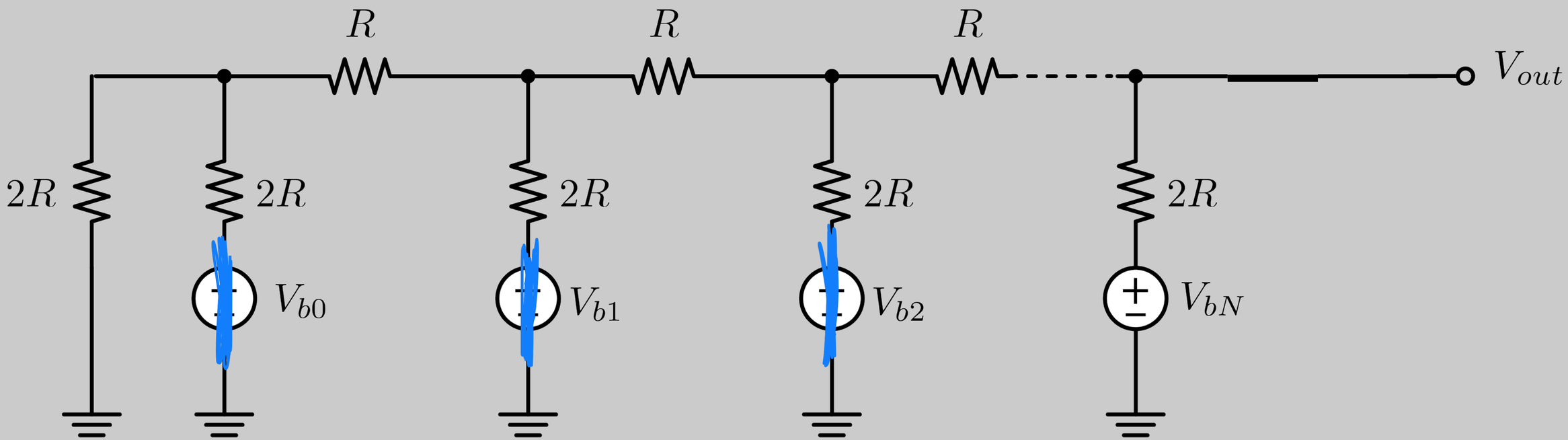
R-2R DAC



1	0	0	1
2^3	2^2	2^1	2^0

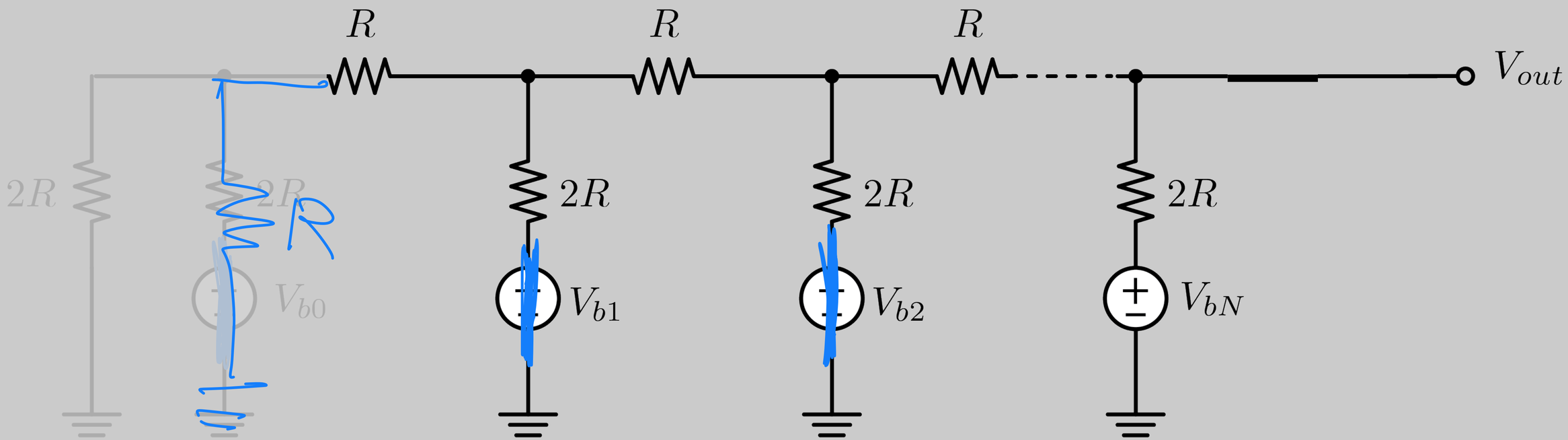
→ 9/16

R-2R DAC

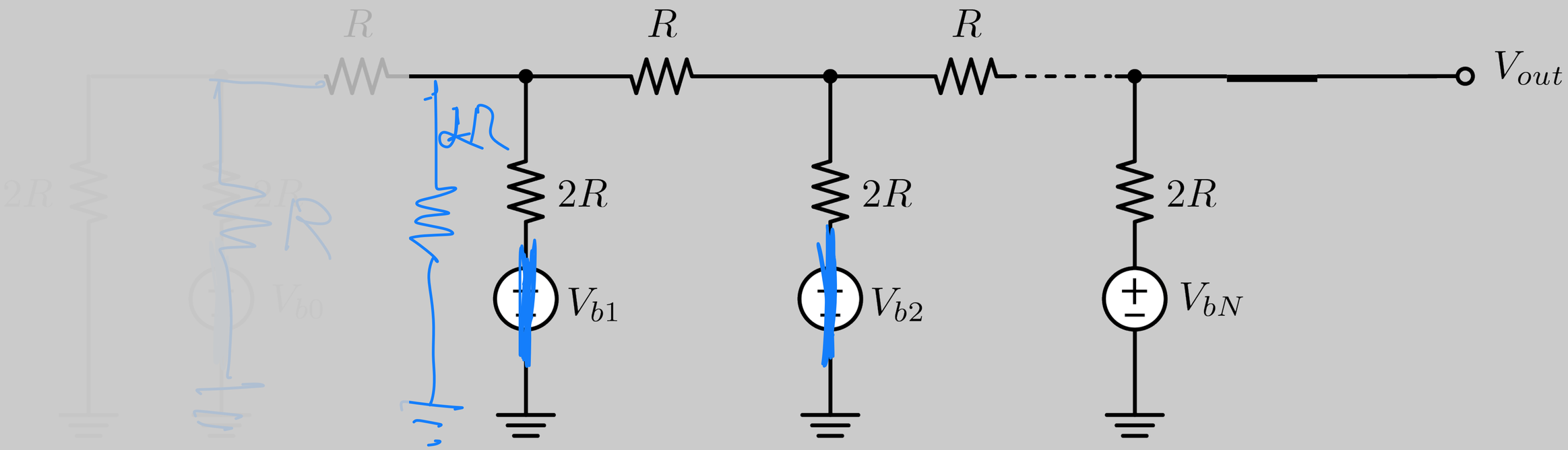


Solve Via Super Position!

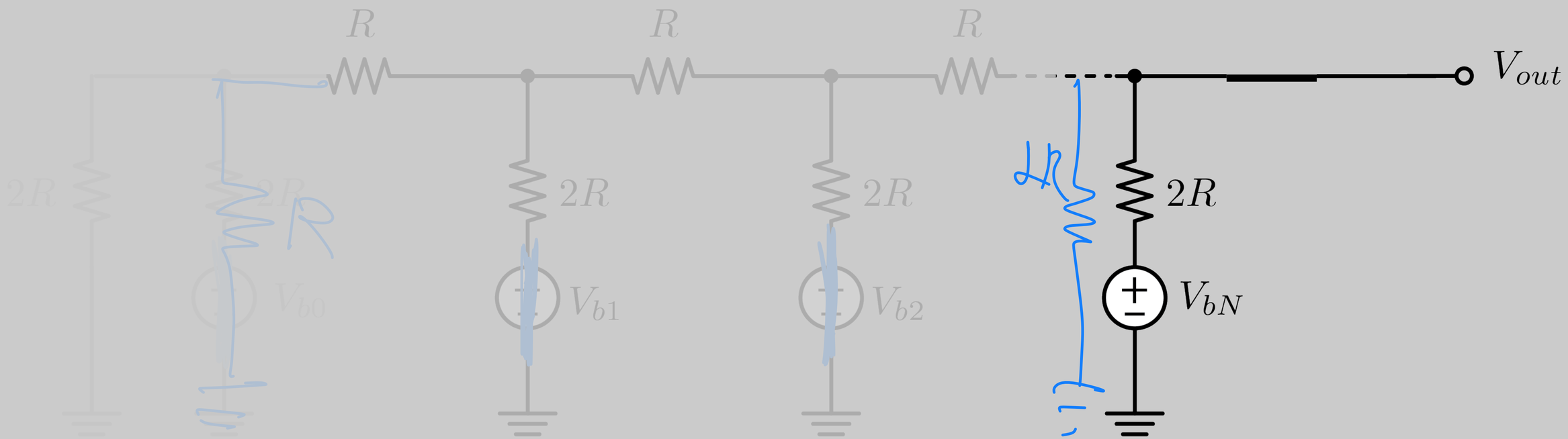
R-2R DAC



R-2R DAC

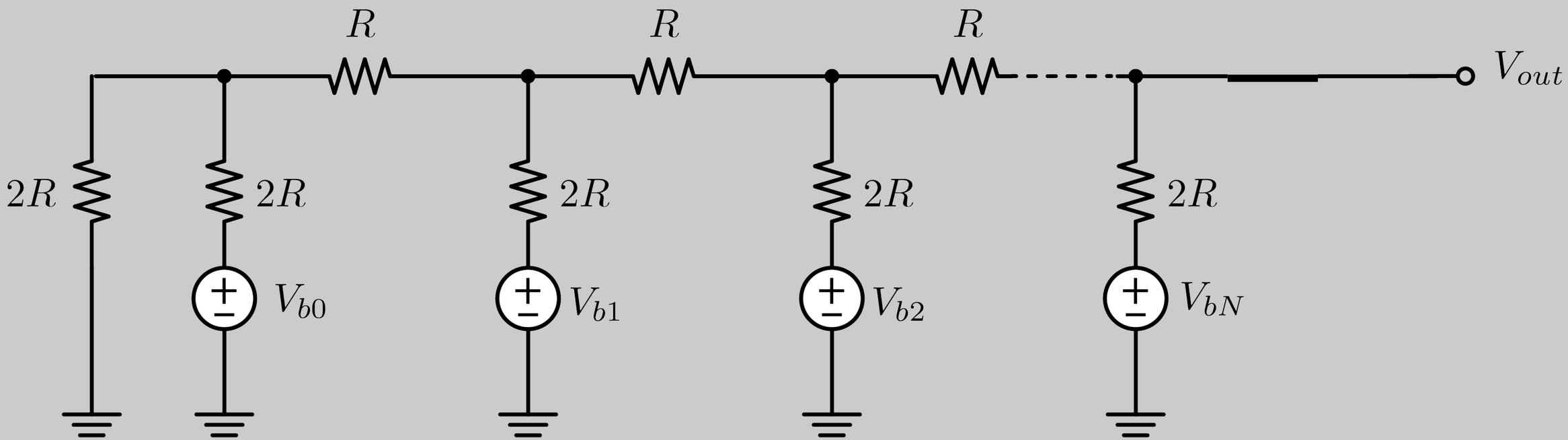


R-2R DAC



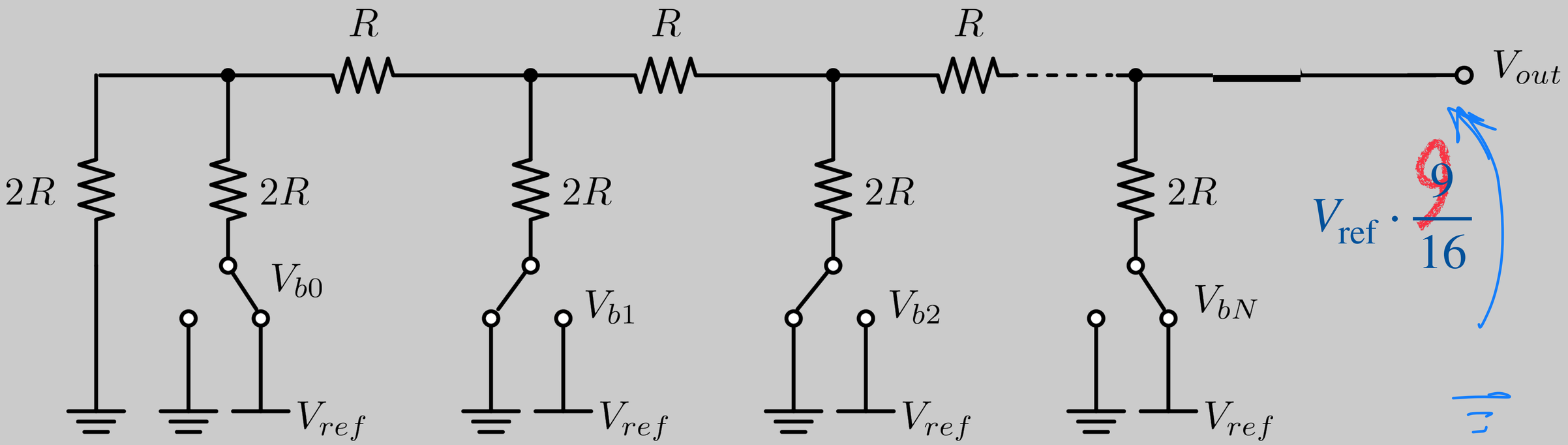
$$V_{\text{out}} = \frac{V_{\text{bN}}}{2}$$

R-2R DAC



$$V_{out} = \frac{V_{b0}}{2^N} + \frac{V_{b1}}{2^{N-1}} + \ldots + \frac{V_{bN}}{2}$$

R-2R DAC

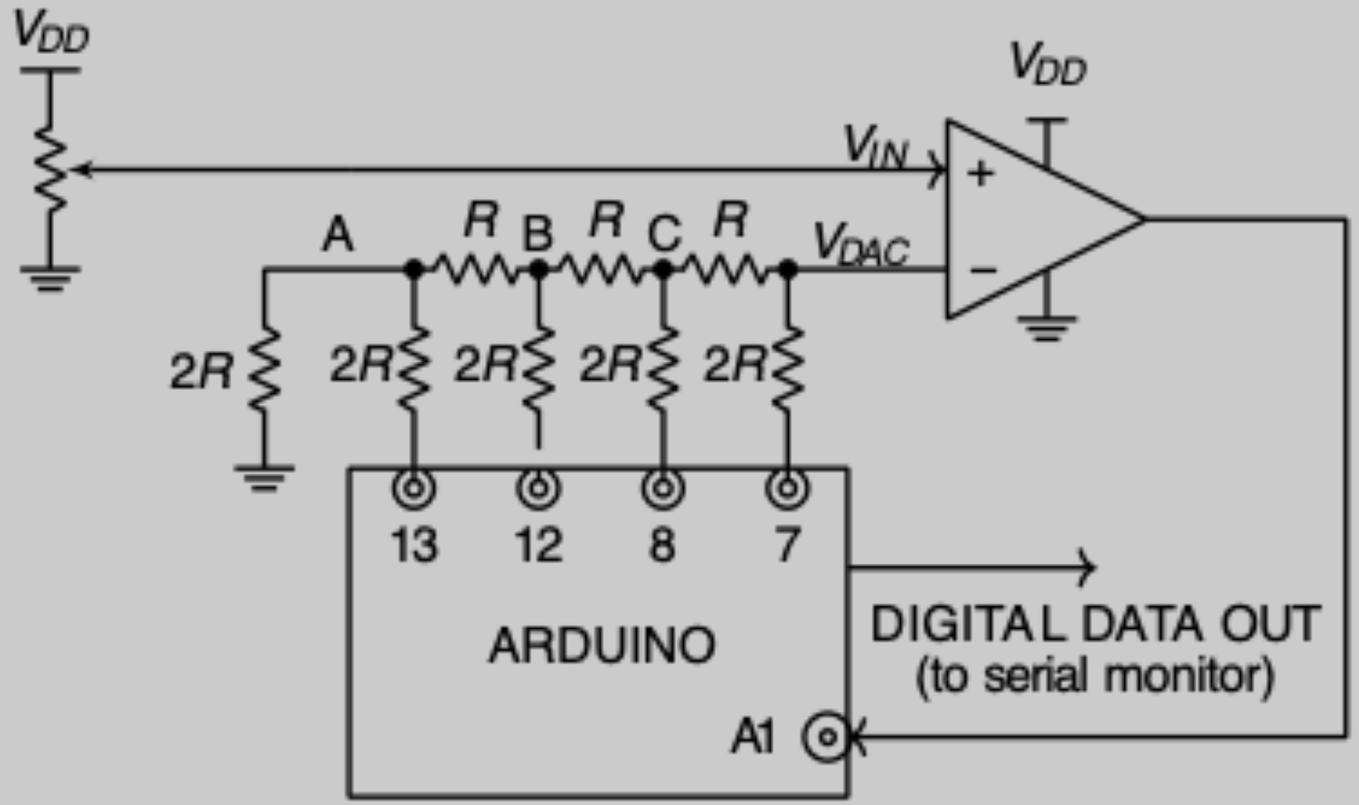


1	0	0	1
2^3	2^2	2^1	2^0

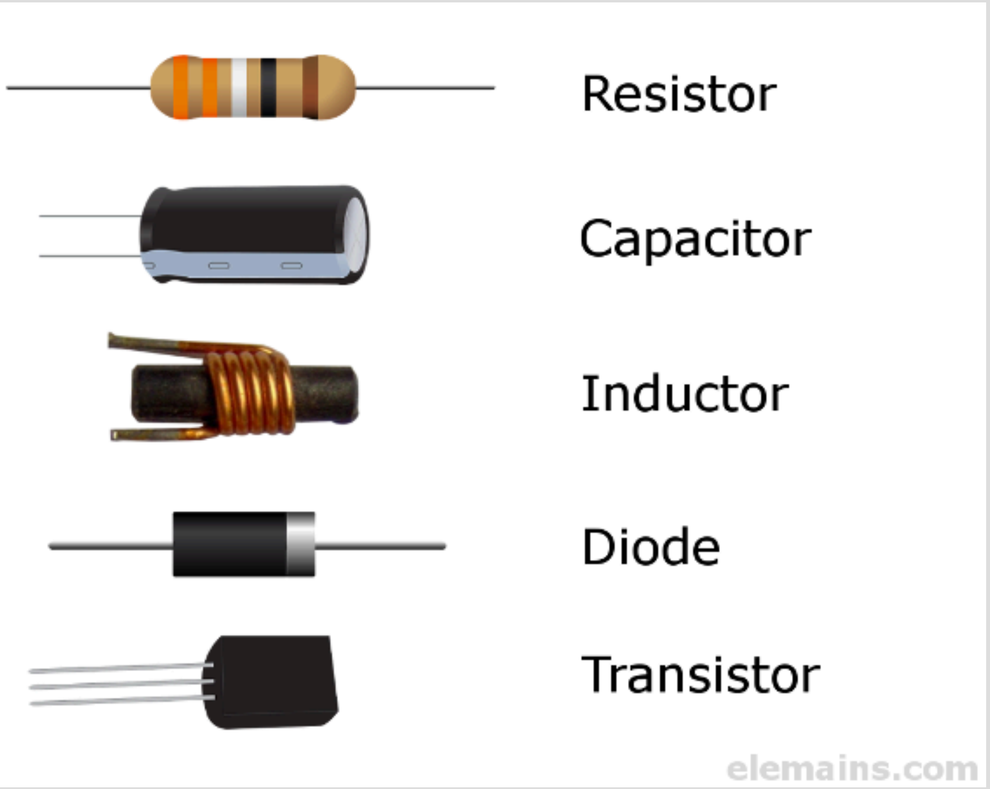
$\rightarrow$ 9/16

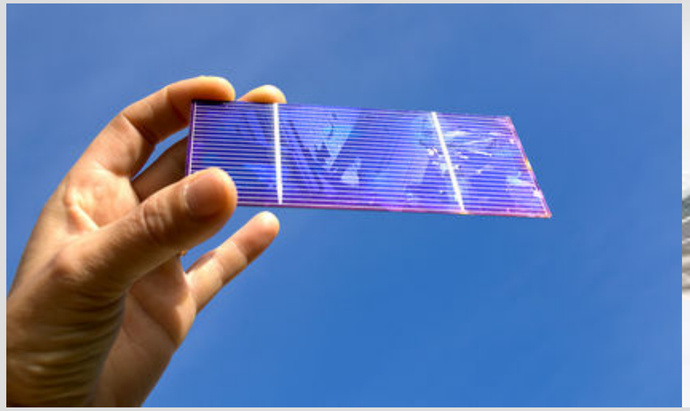
Lab 2: SAR ADC

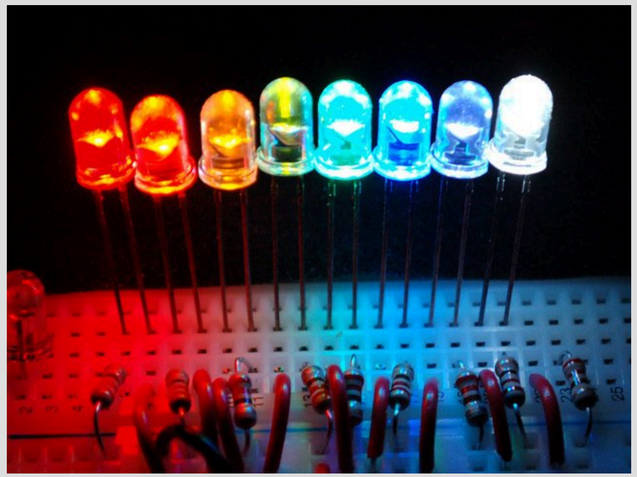
- Successive Approximation Resistor
- Use DAC to guess bit by bit
- Iterate (log(N)) times



Devices as part of a system

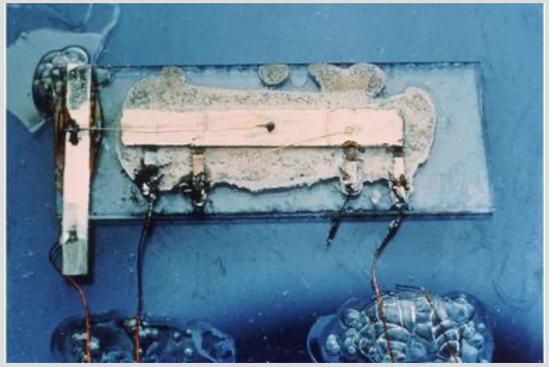




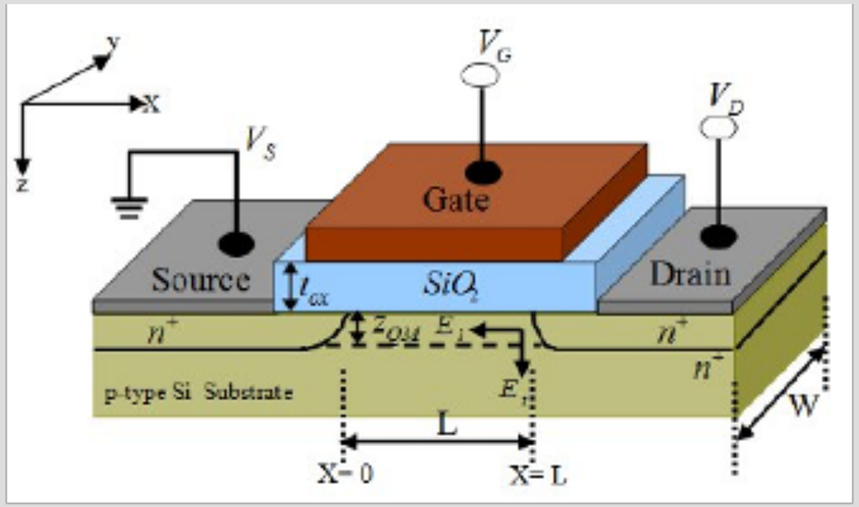


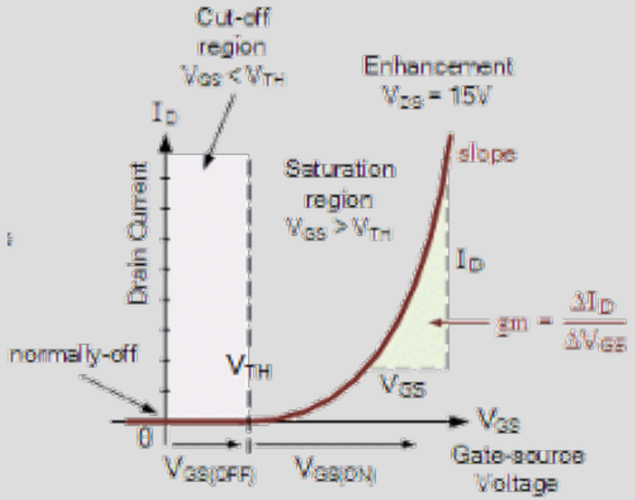
Transistor

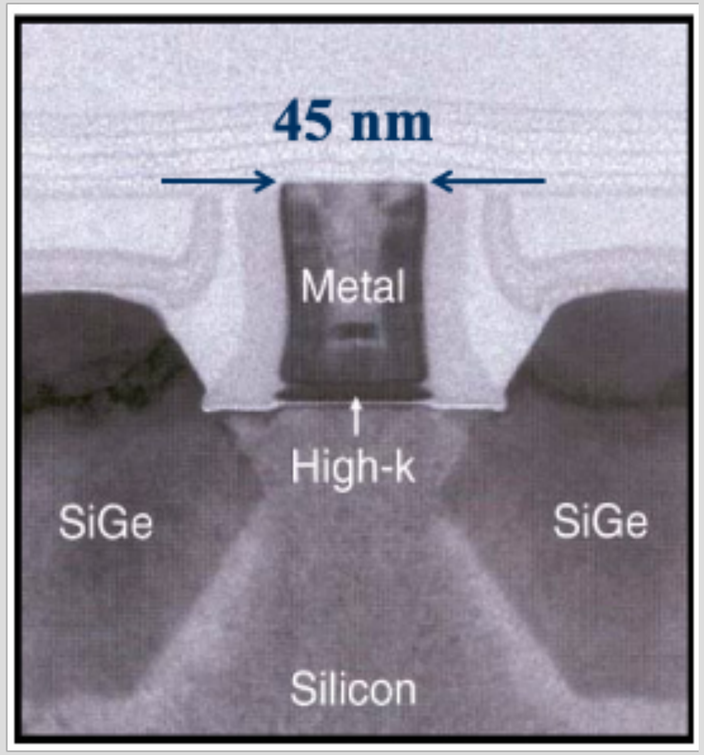
First transistor – Dec 1947



First integrated circuit 1958

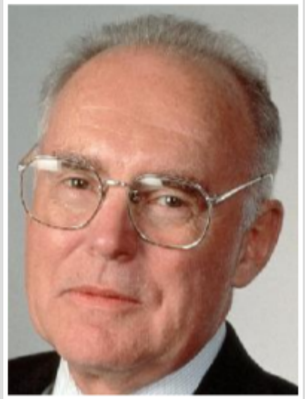






Computational advances due to fabrication advances

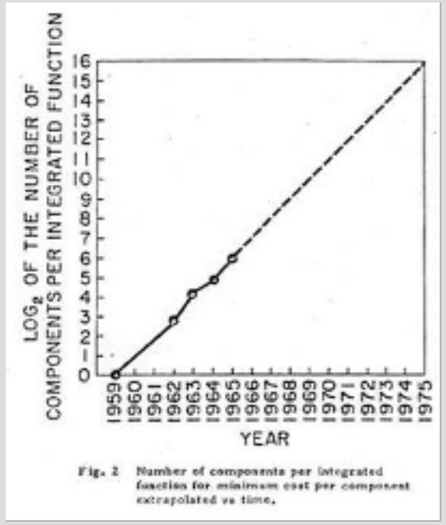
Moore's law is the observation that the number of [transistors in a dense integrated circuit doubles approximately every two years.]



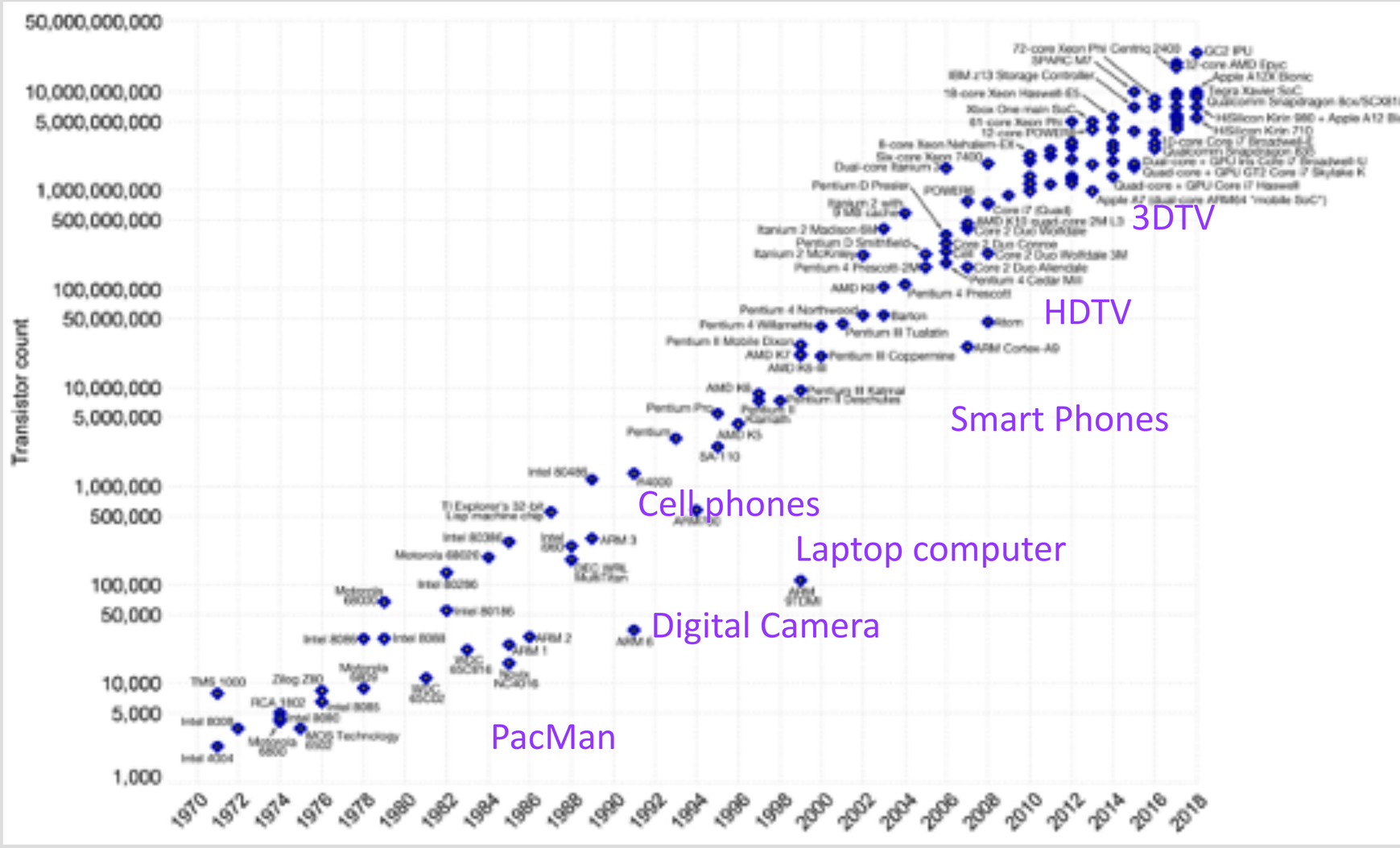
Gordon Moore

Intel Cofounder

B.S. Cal 1950!



Electronics Magazine, 1965



FinFET

FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

***Abstract*—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.**

***Index Terms*—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.**

I. Introduction

TO DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because

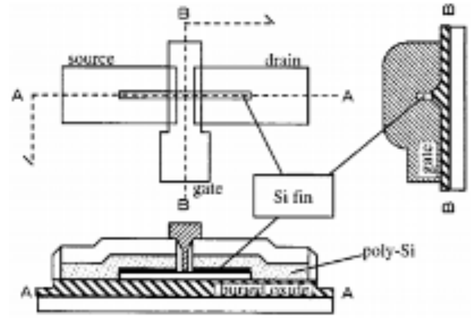


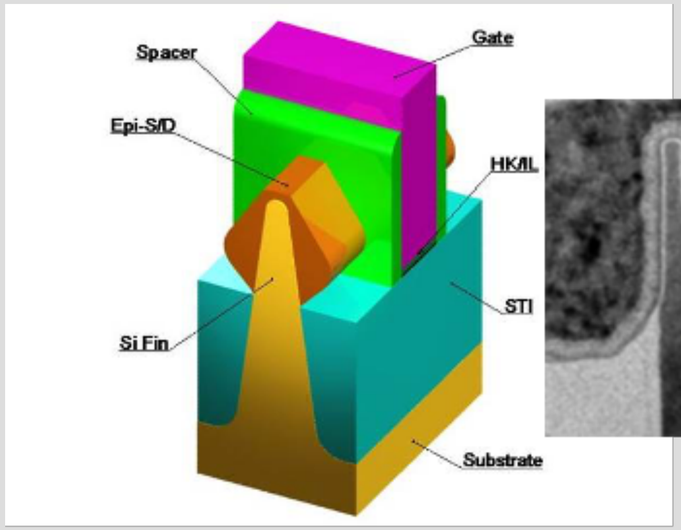
Fig. 1. FinFET typical layout and schematic cross sectional structures.

Prof. Tsu-Jae King Liu

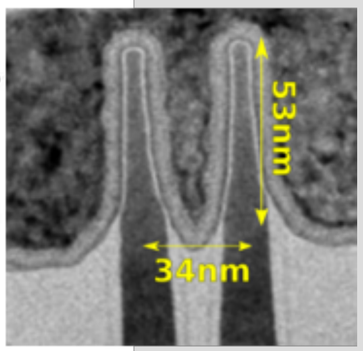
Prof. Jeff Bokor

Prof. Chenming Hu (left)

Go Bears!

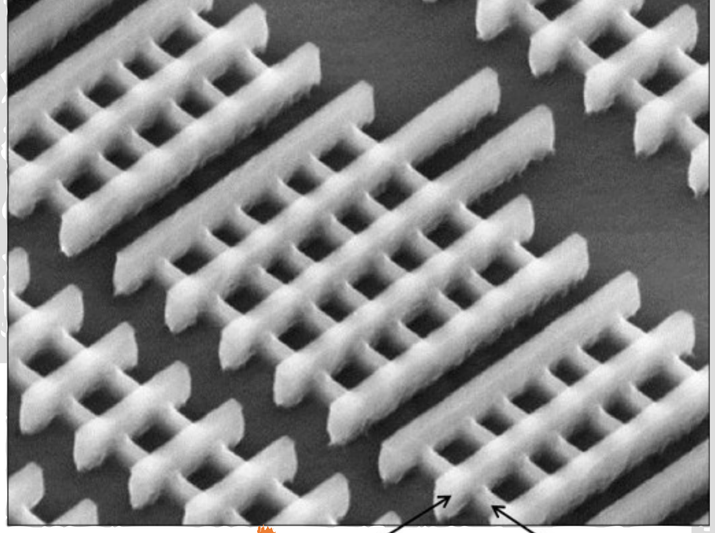


source: Chinese Academy of Microelectronics



source: Intel

Sense of Scale



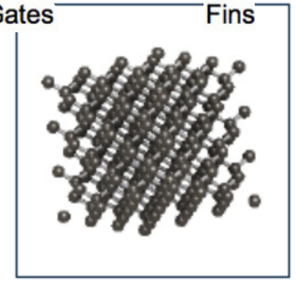
Mark
1.66 m

Fly
7 mm

Mite
300 um

Blood Cell
7 um

Virus
100 nm



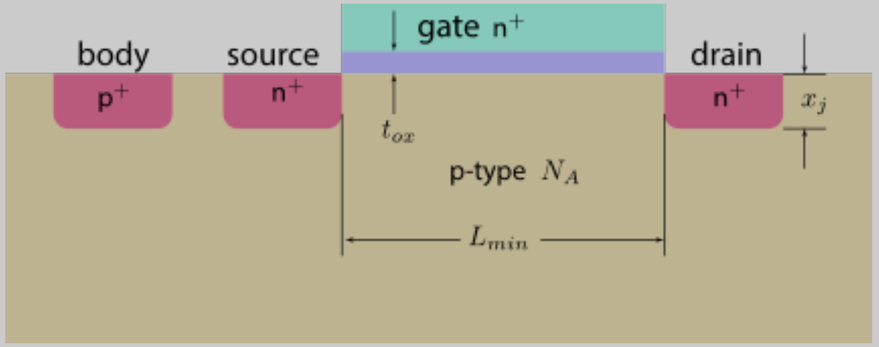
Silicon Atom
0.24 nm

10 1 100 10 1 100 10 1 100 10 1 0.1

meter | millimeter | micrometer | nanometer

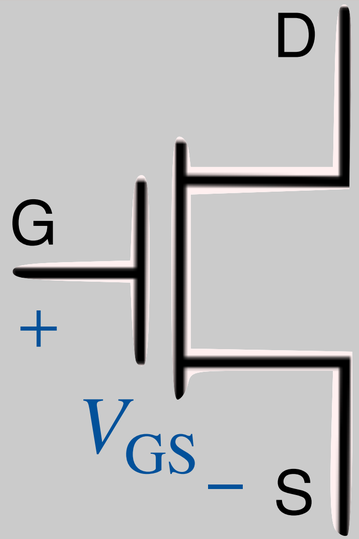
Source: Mark Bohr, IDF14

MOS Transistor

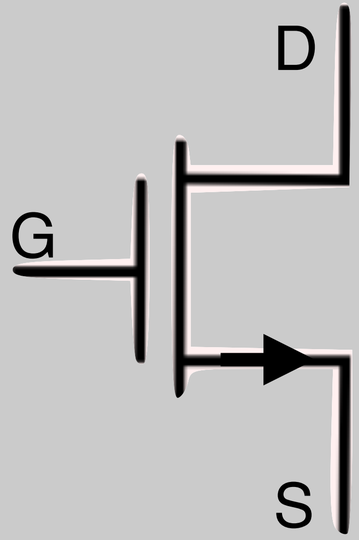


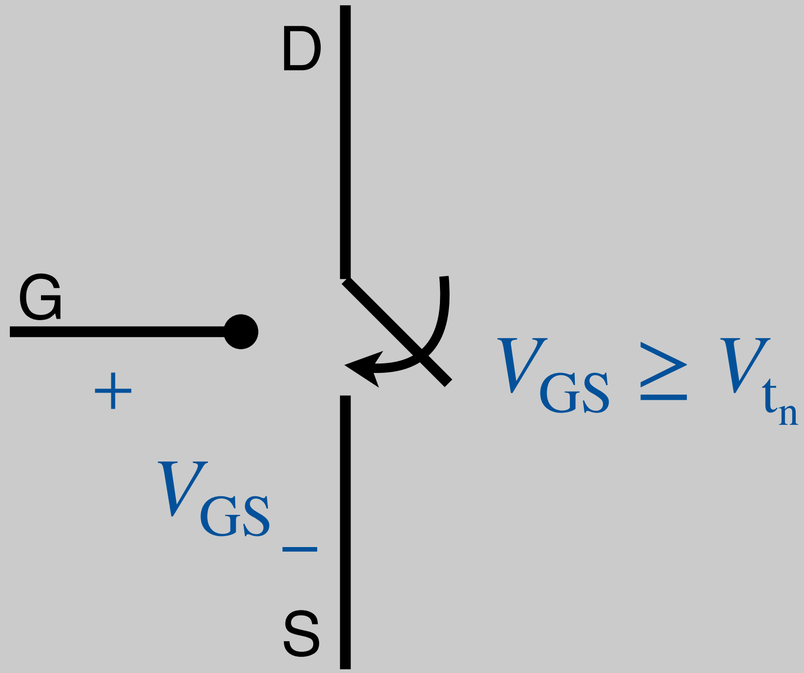
- MOS: metal-oxide-semiconductor
- MOSFET: MOS field effect Transistor
- Two kinds:
  - NMOS - current carried by electrons
  - PMOS - current carried by “holes” (lack of e)

Simplest Circuit Model of NMOS



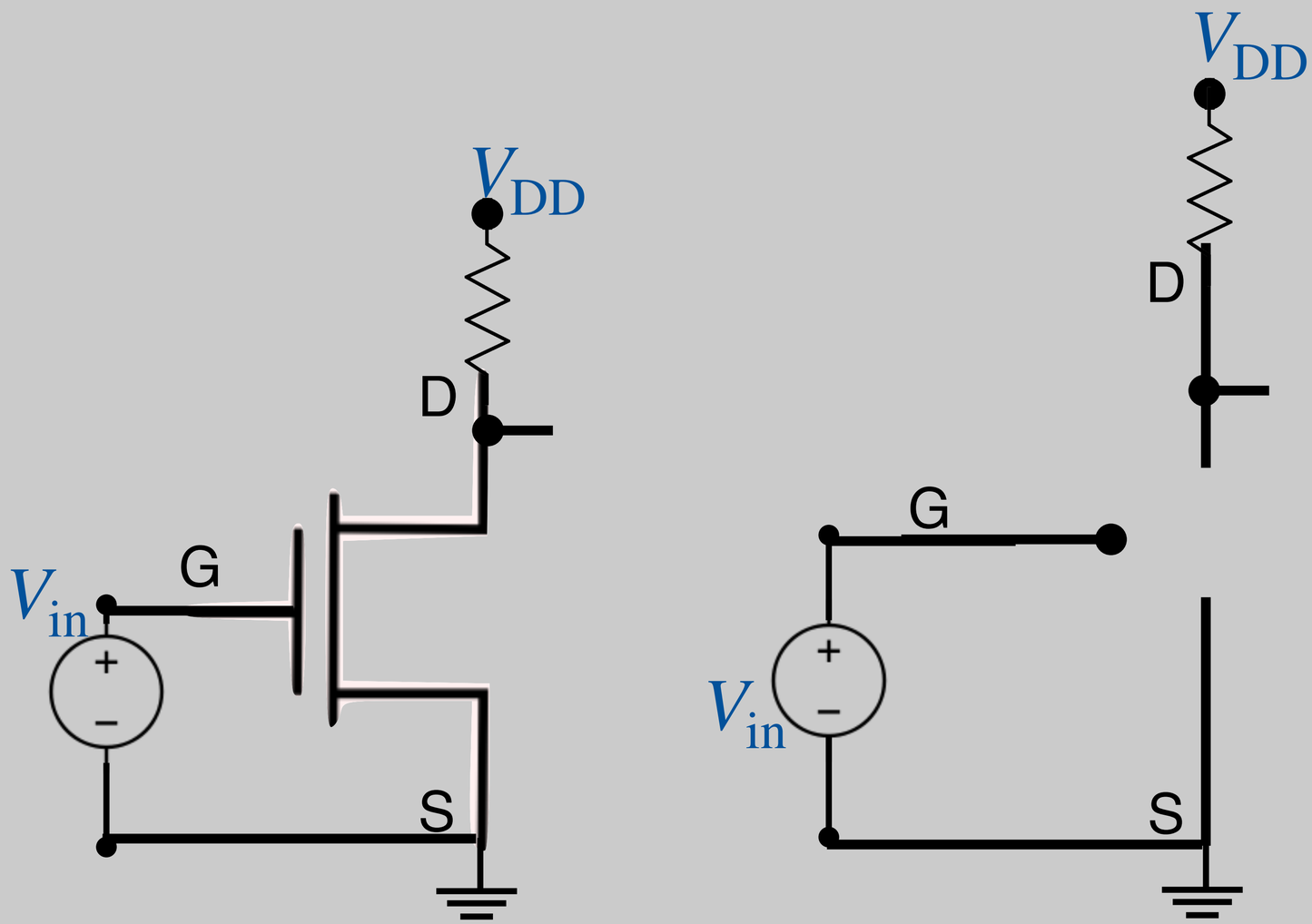
Or:





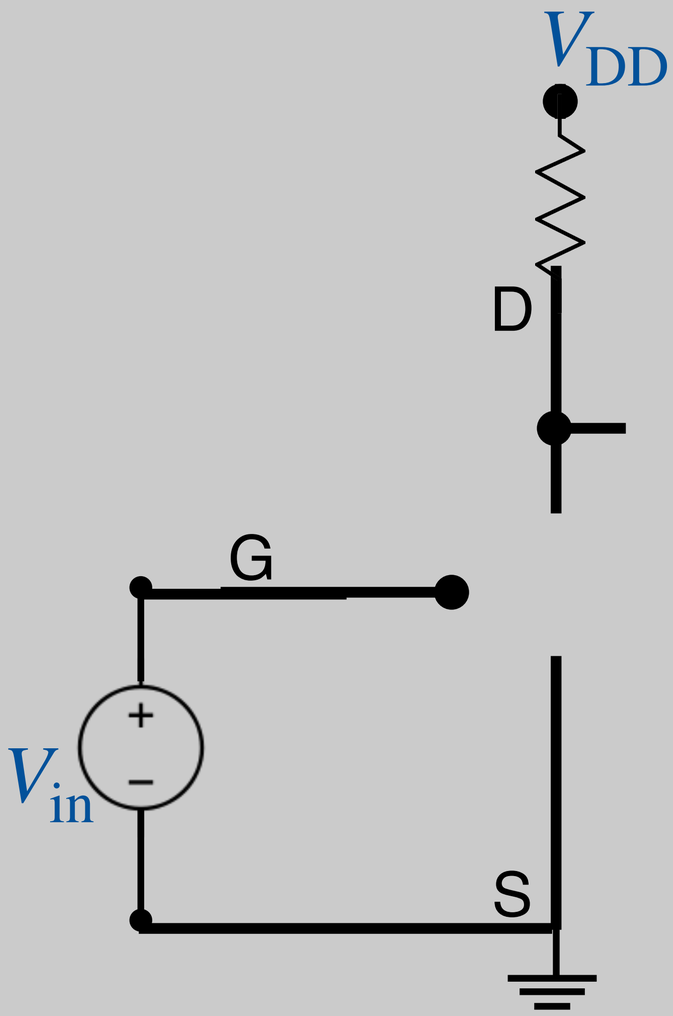
Simplest Circuit Model of NMOS

$V_{GS} < V_{t_n}$

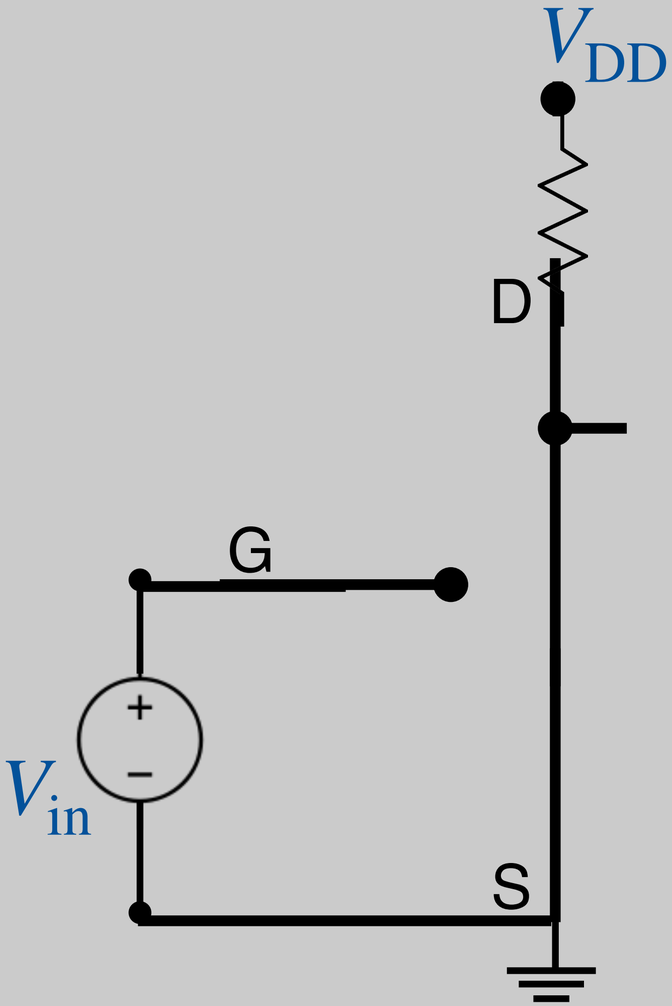


Simplest Circuit Model of NMOS

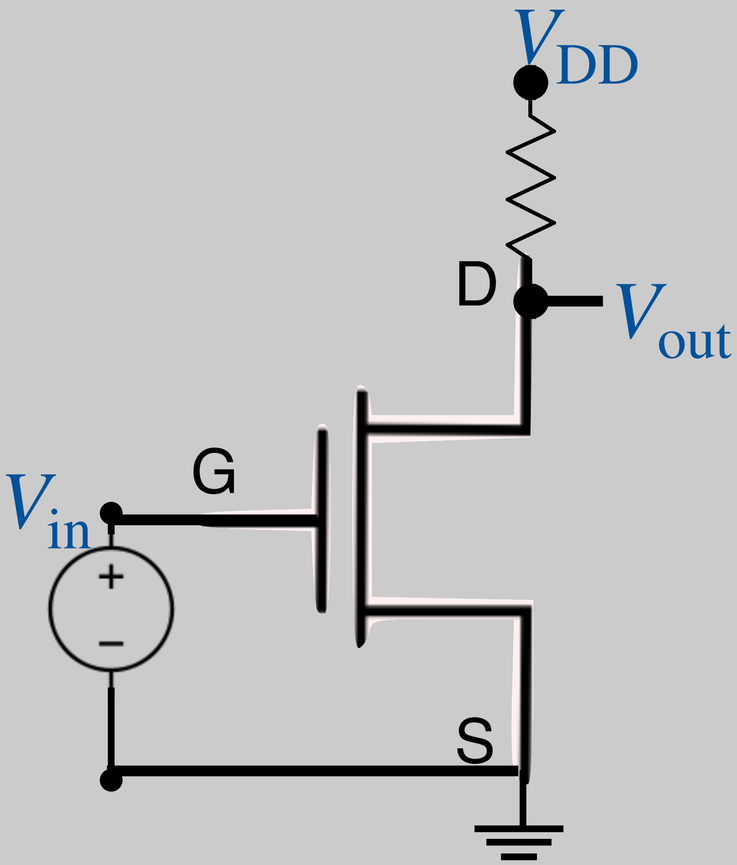
$V_{GS} < V_{t_n}$

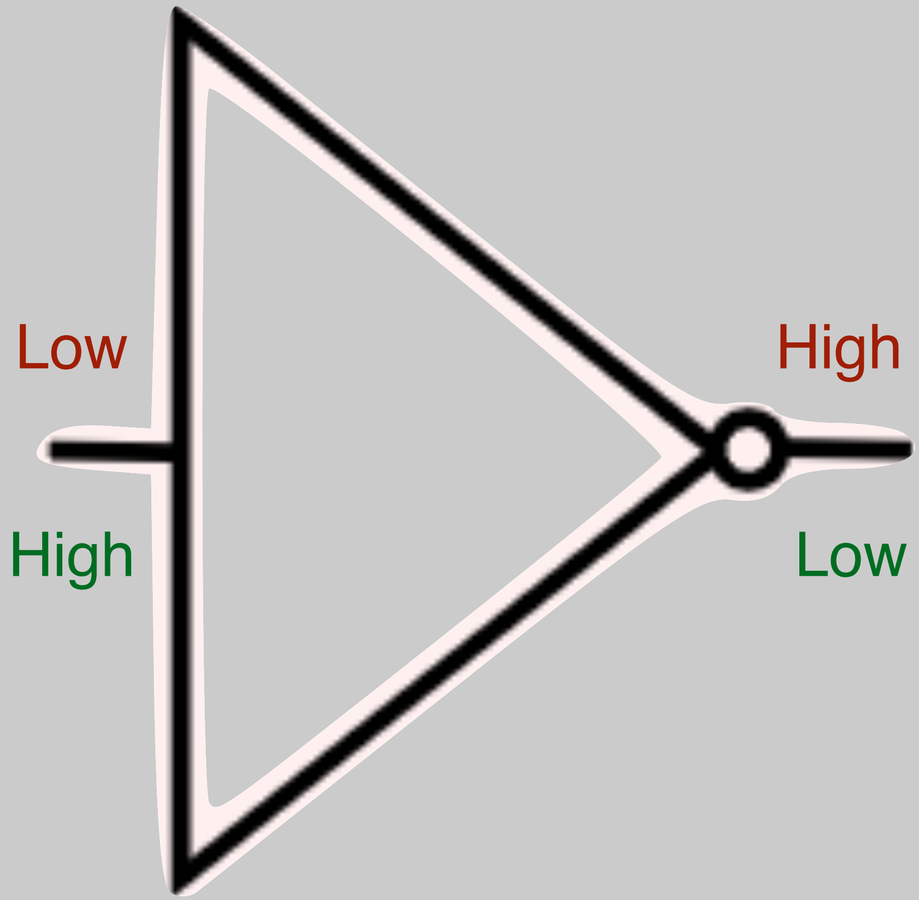


$V_{GS} \geq V_{t_n}$

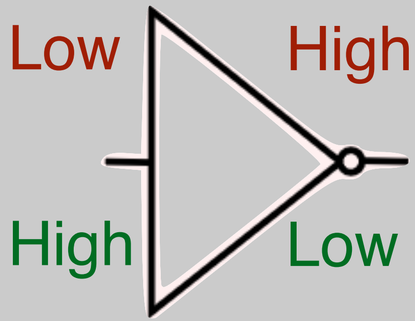


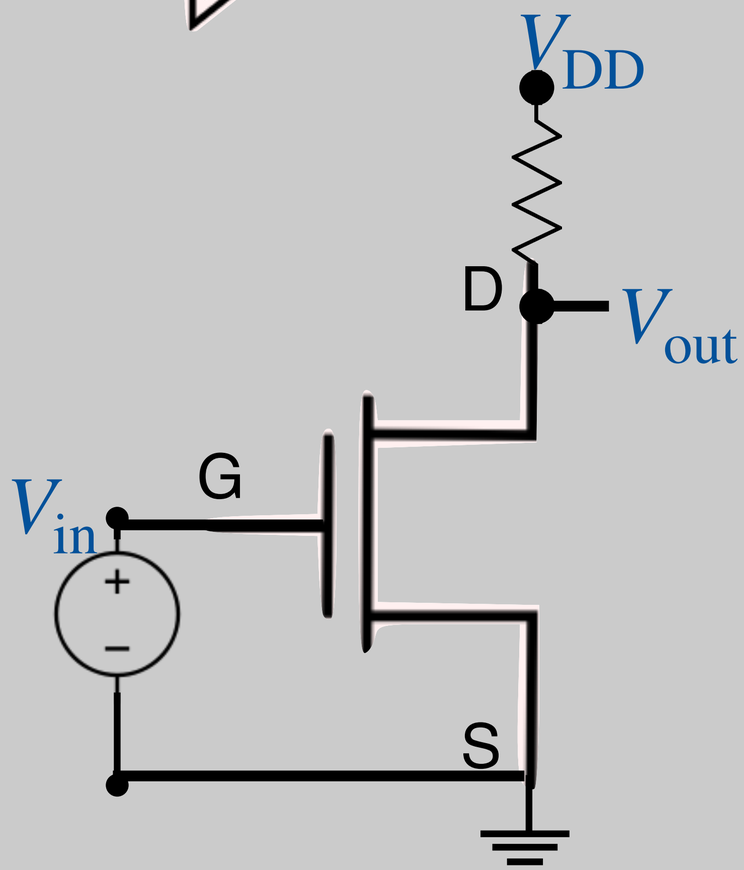
Simple NMOS Inverter



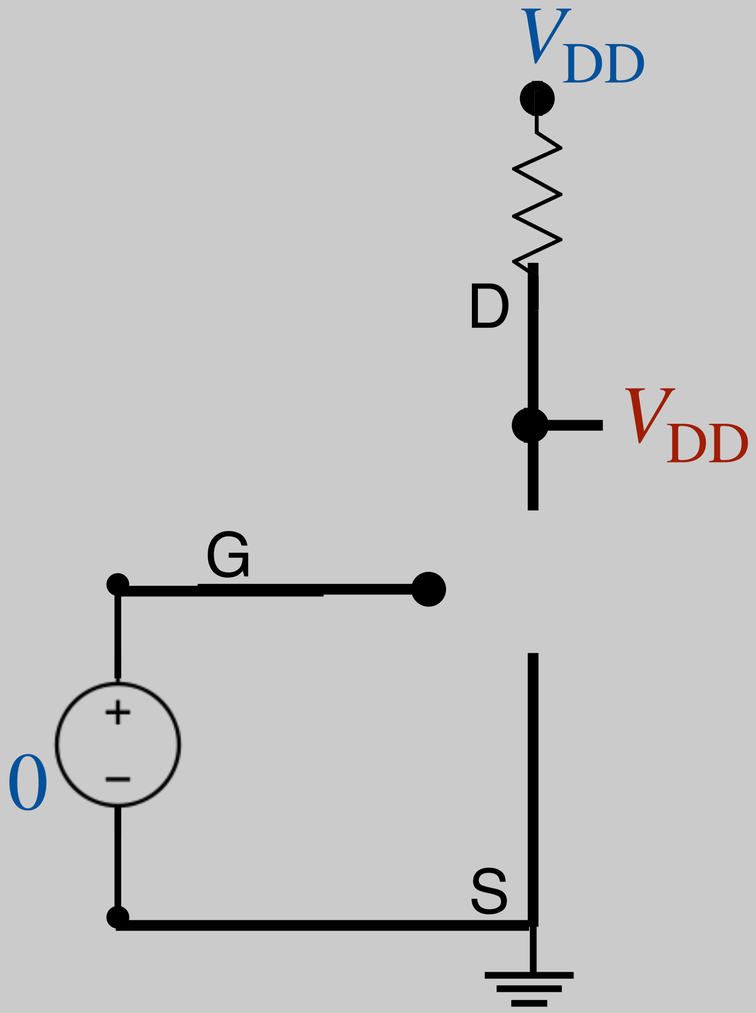


Simple NMOS Inverter

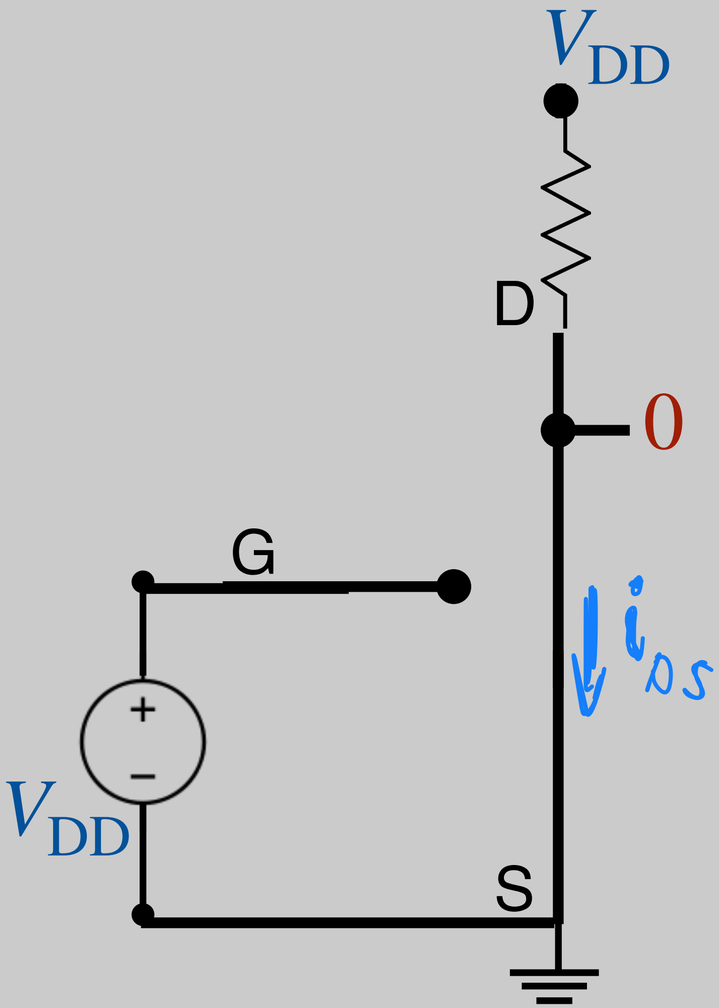




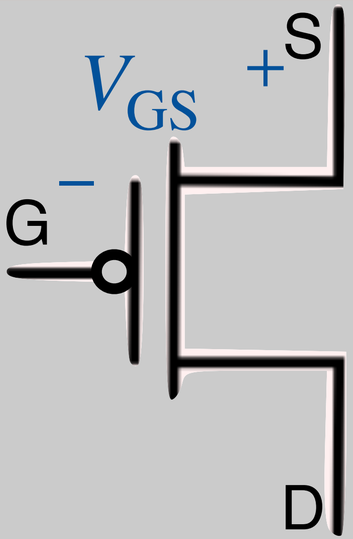
$V_{GS} < V_{t_n}$



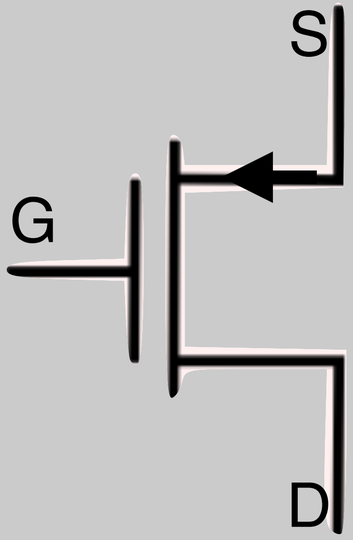
$V_{GS} \geq V_{t_n}$

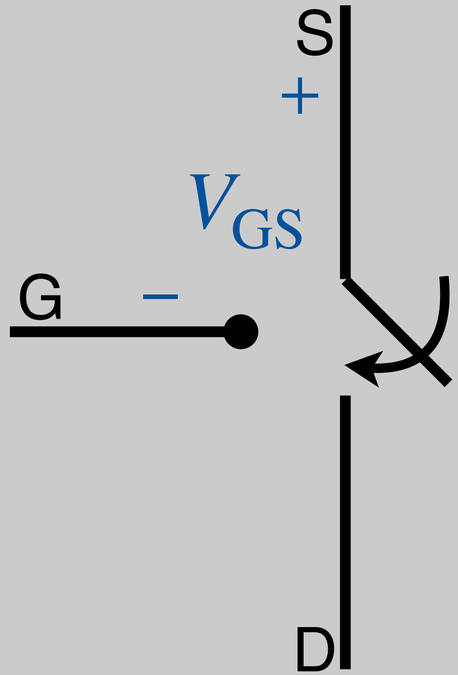


Simplest Circuit Model of PMOS



Or:

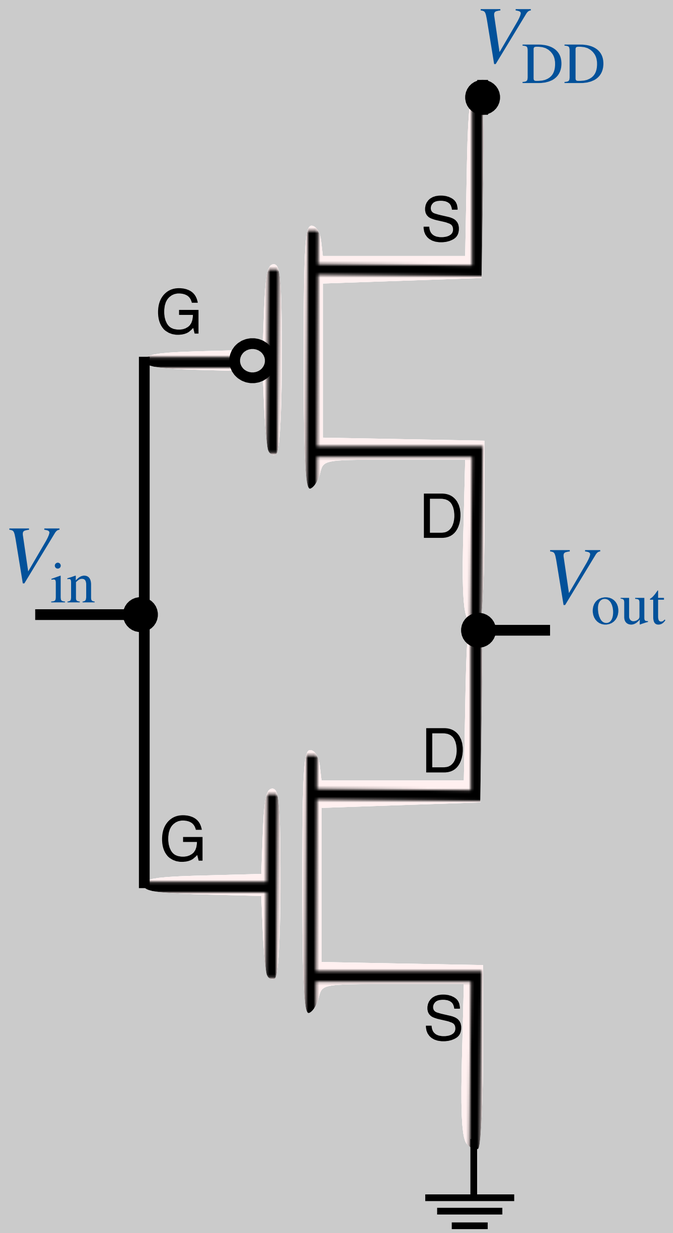




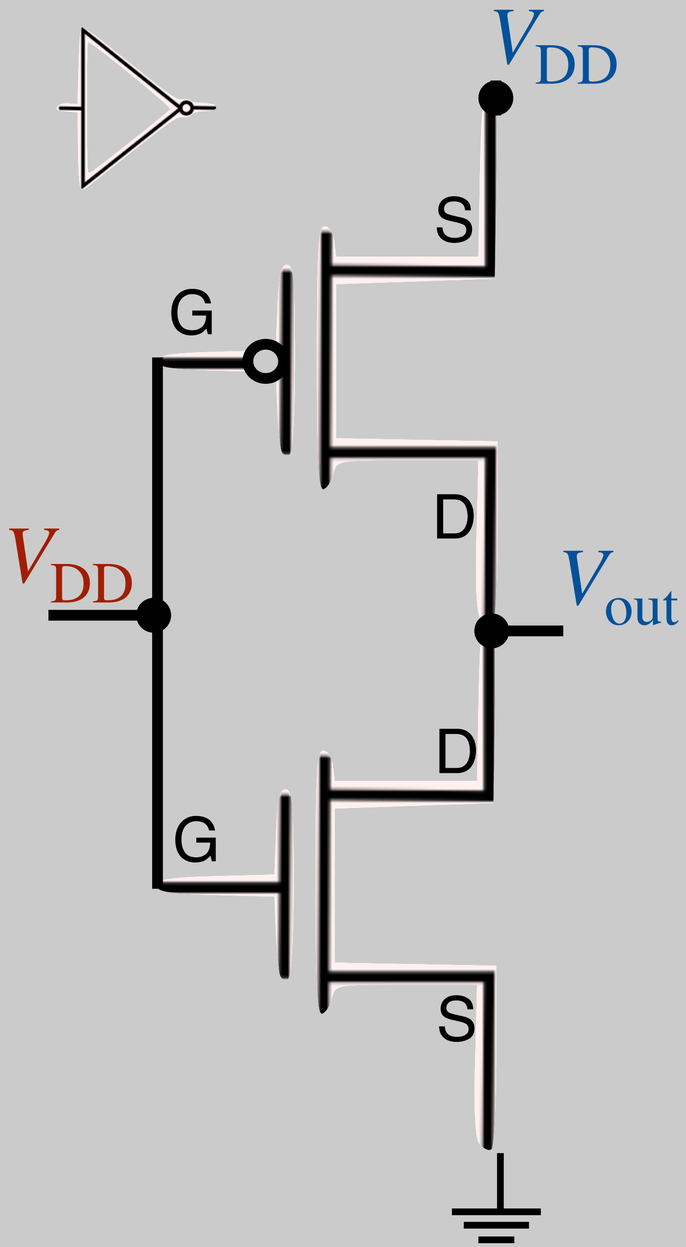
$$V_{GS} \leq -|V_{t_p}|$$

CMOS (Complementary MOS)

- PMOS + NMOS
- Very low power consumption inverter
- Dominant technology



CMOS (Complementary MOS)



$V_{in} = V_{DD} \quad \Rightarrow'' 1''$

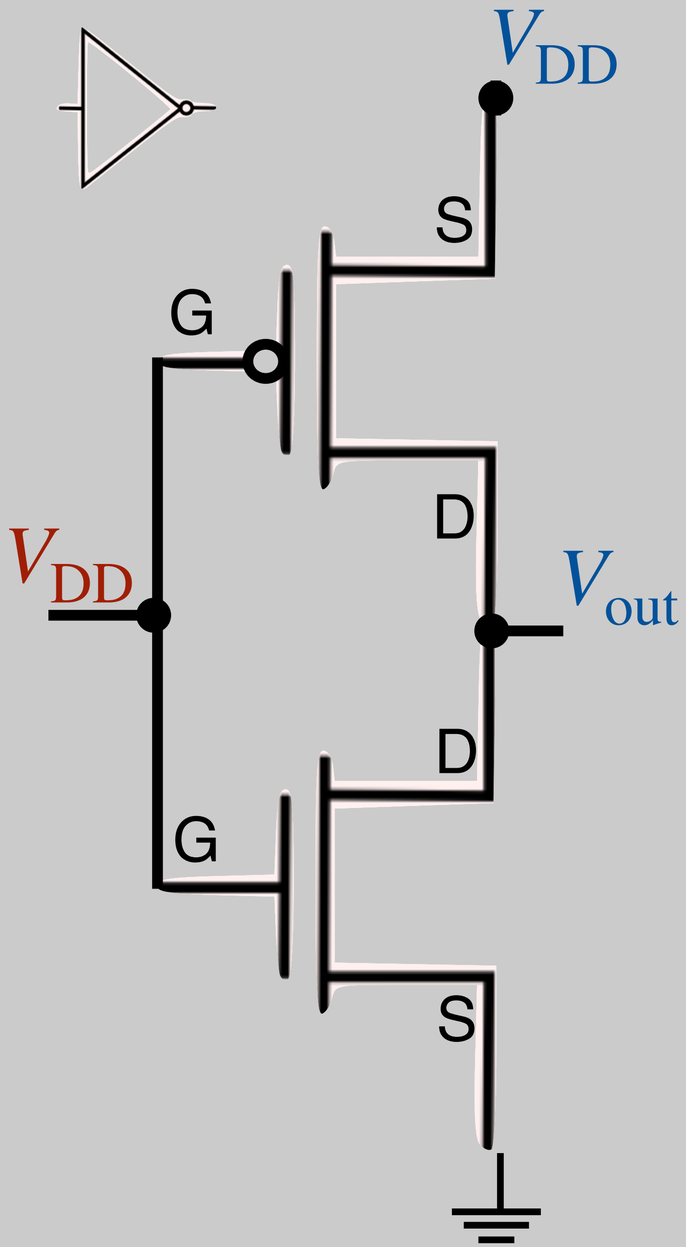
PMOS: $V_{GS} = 0 \quad > -|V_{t_p}|$

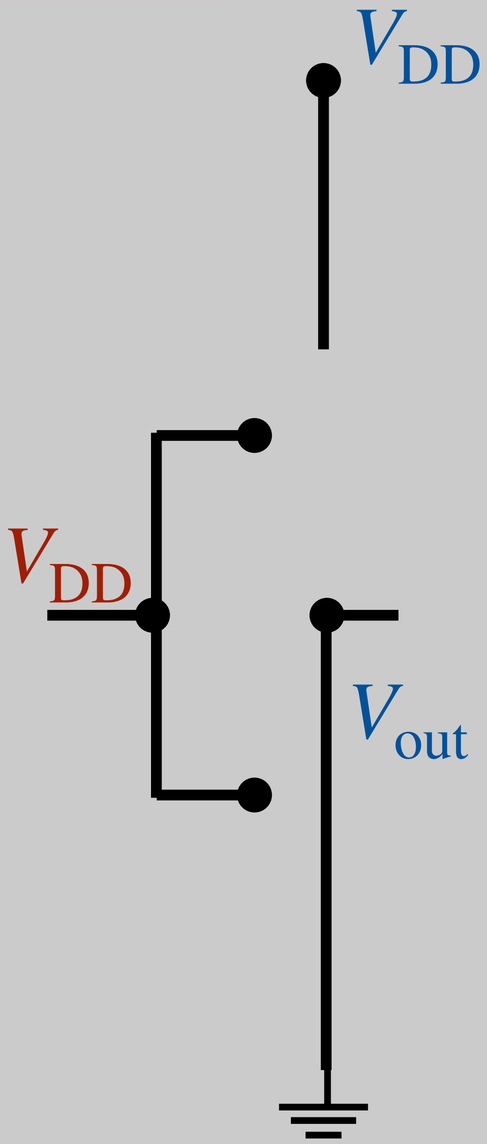
$\Rightarrow$Off, open circuit

NMOS: $V_{GS} = V_{DD} > V_{t_n}$

$\Rightarrow$On, short circuit

CMOS (Complementary MOS)





$V_{in} = V_{DD} \Rightarrow "1"$

PMOS: $V_{GS} = 0 > -|V_{t_p}|$

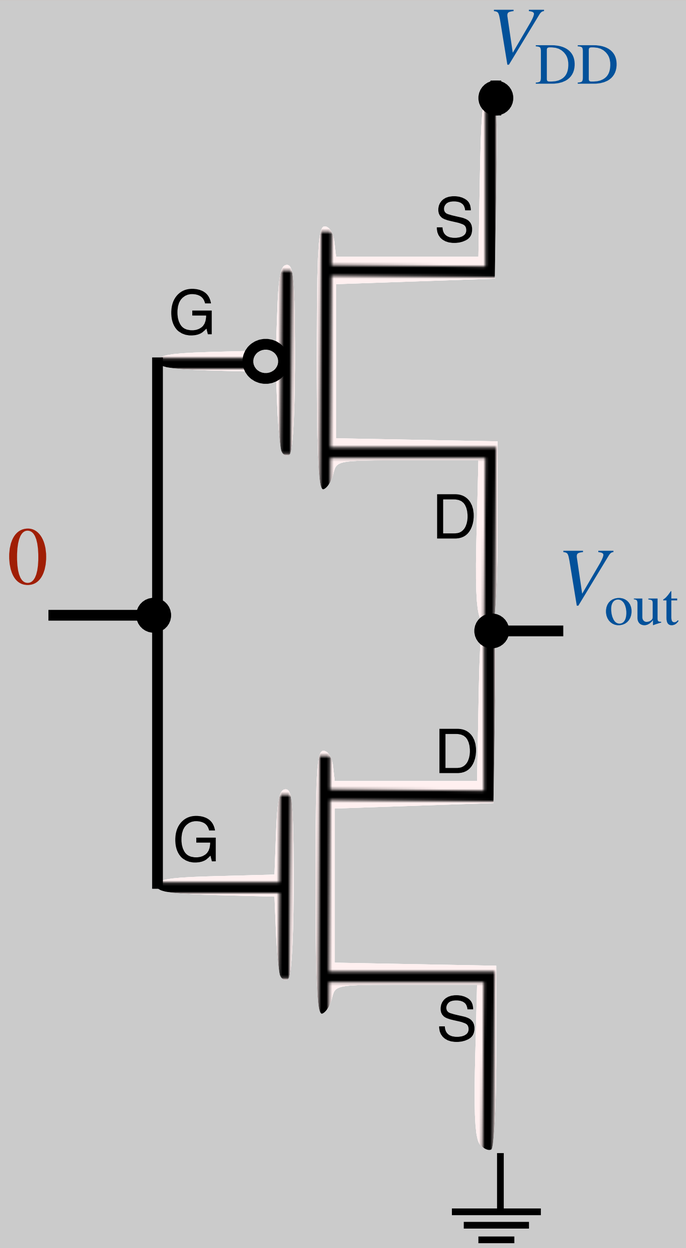
$\Rightarrow$Off, open circuit

NMOS: $V_{GS} = V_{DD} > V_{t_n}$

$\Rightarrow$On, short circuit

$V_{out} = 0V \Rightarrow "0"$

CMOS (Complementary MOS)



$V_{in} = 0 \quad \Rightarrow'' 0''$

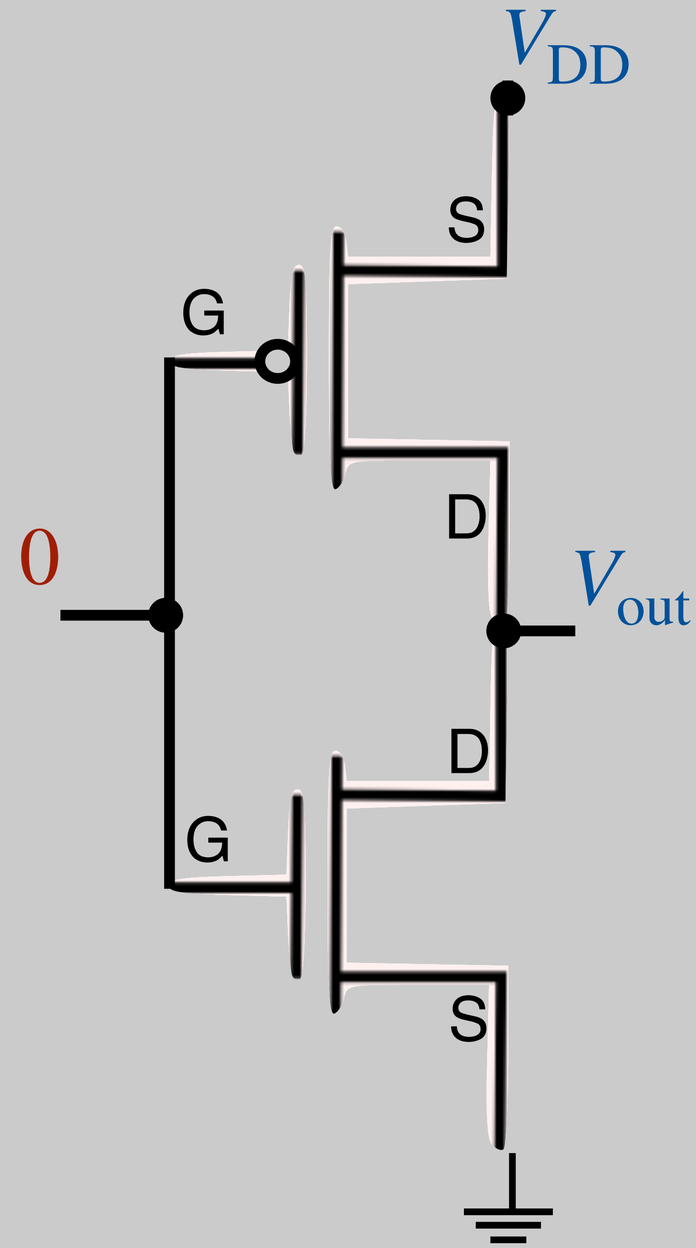
PMOS: $V_{GS} = -V_{DD} < -|V_{t_p}|$

$\Rightarrow$On, short circuit

NMOS: $V_{GS} = 0 < V_{t_n}$

$\Rightarrow$Off, open circuit

CMOS (Complementary MOS)



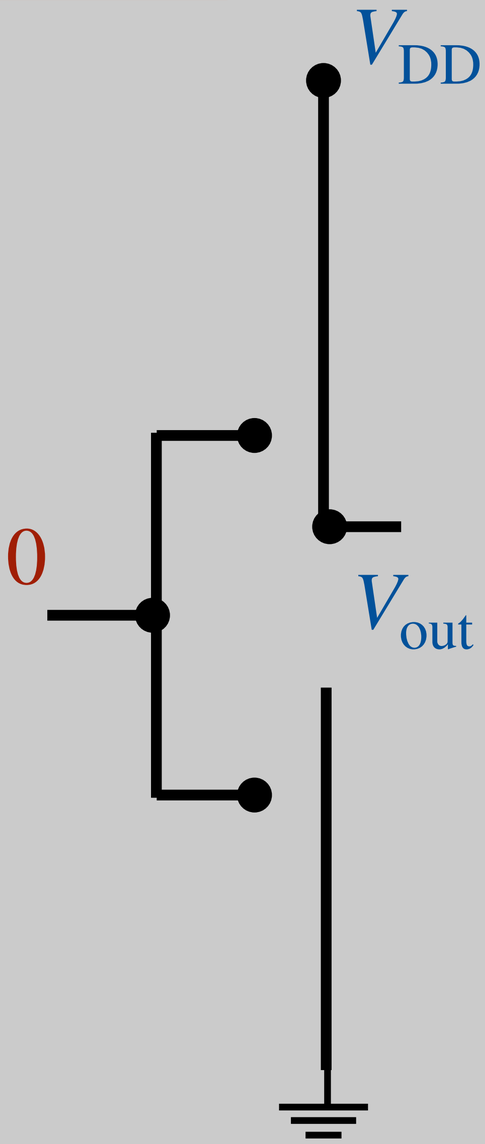
$V_{in} = 0 \quad \Rightarrow "0"$

PMOS: $V_{GS} = -V_{DD} < -|V_{t_p}|$

$\Rightarrow$On, short circuit

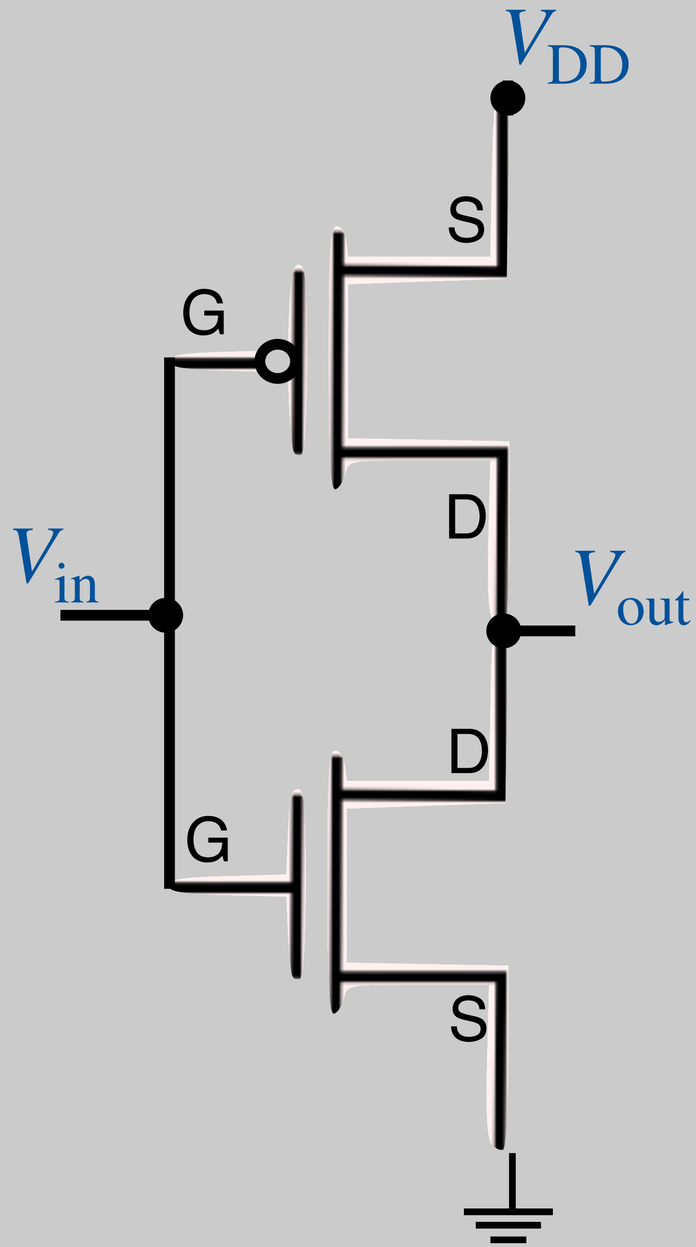
NMOS: $V_{GS} = 0 < V_{t_n}$

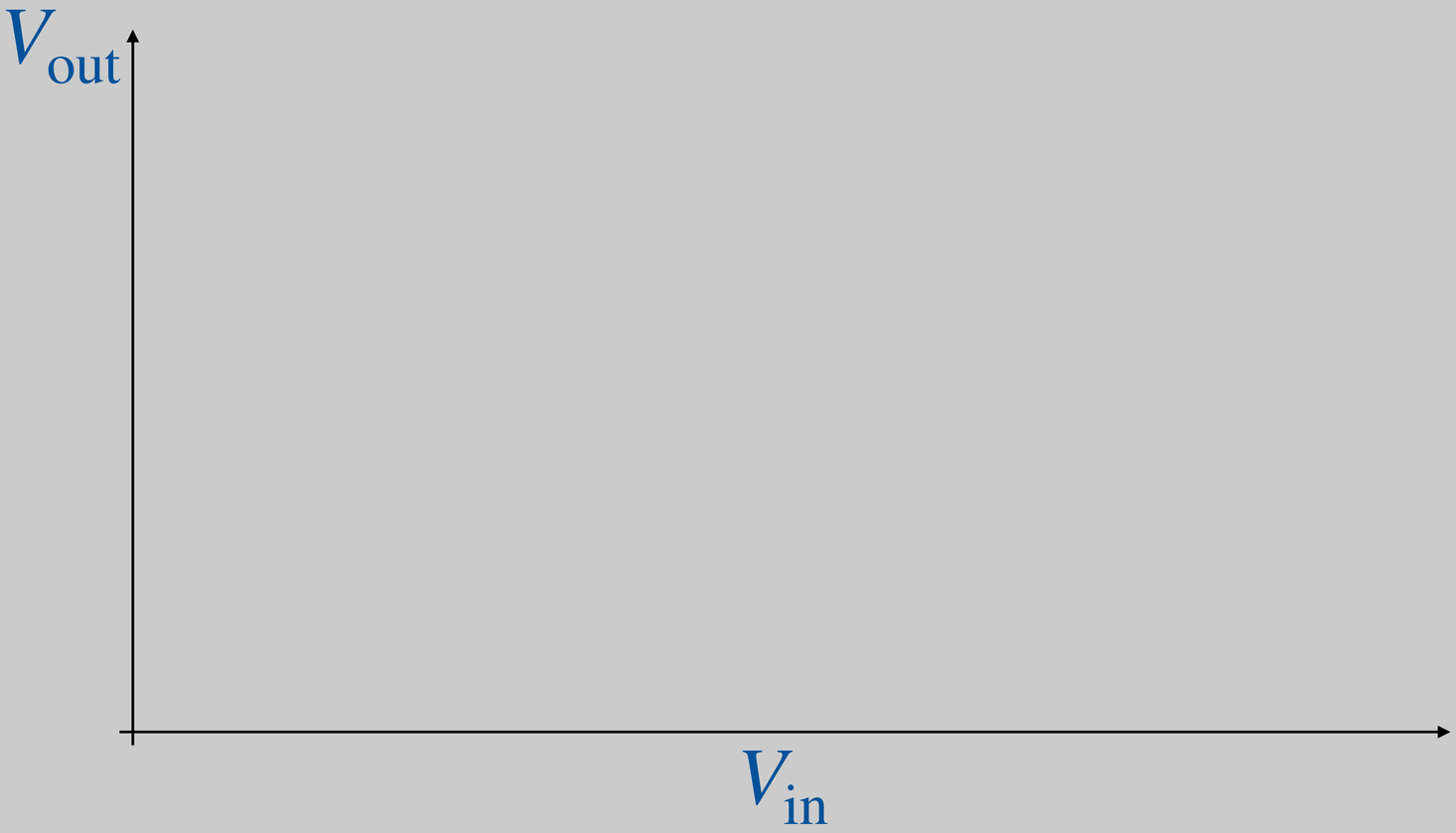
$\Rightarrow$Off, open circuit



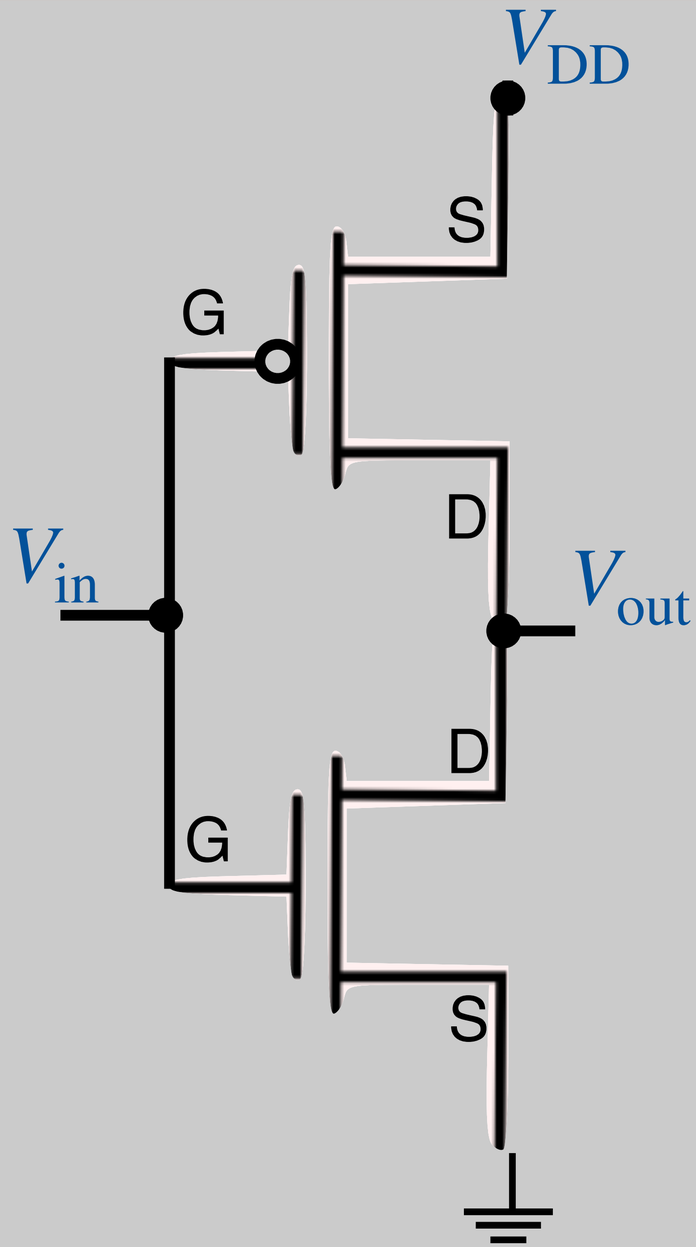
$V_{out} = V_{DD} \Rightarrow "1"$

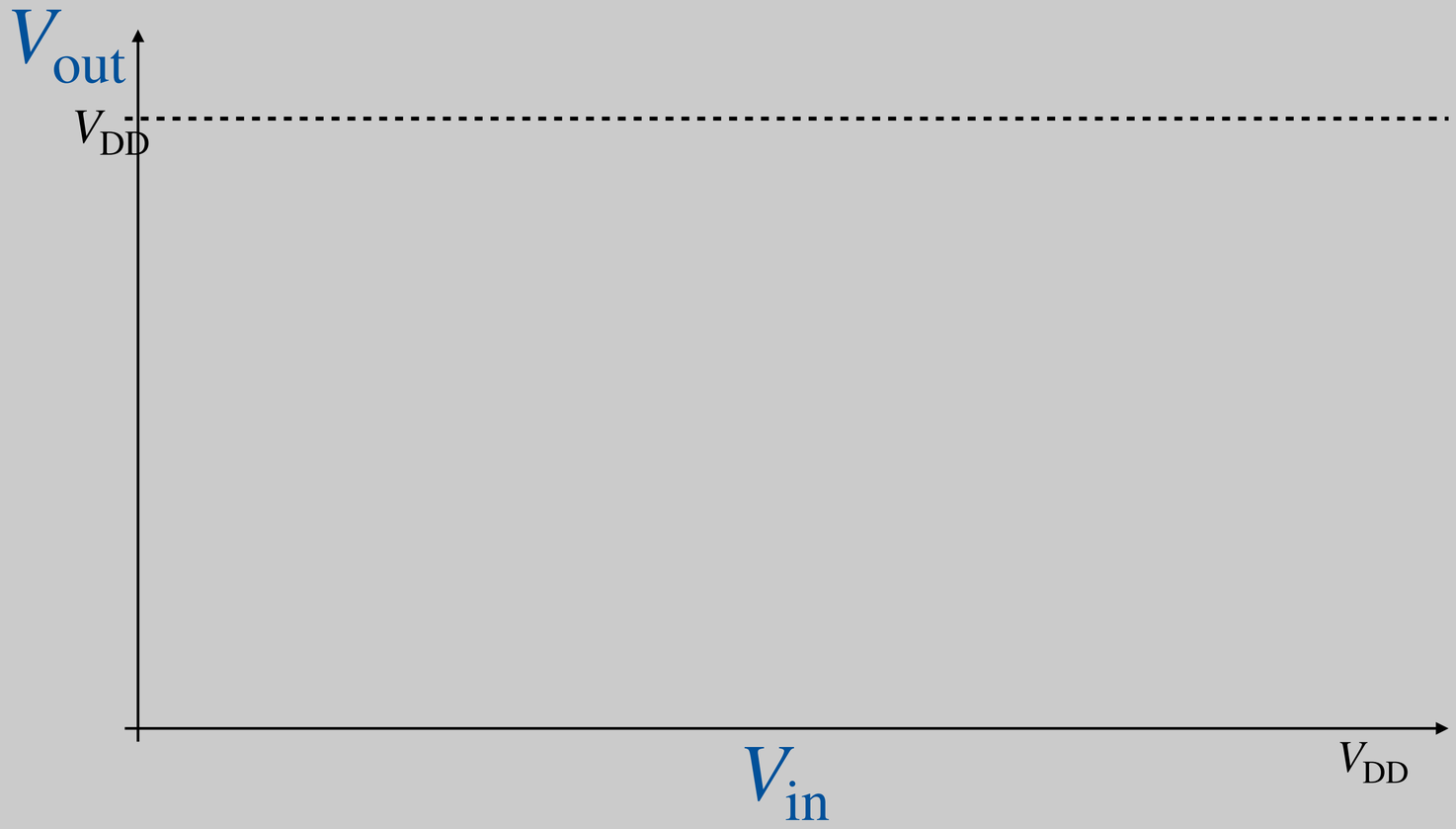
CMOS (Complementary MOS)



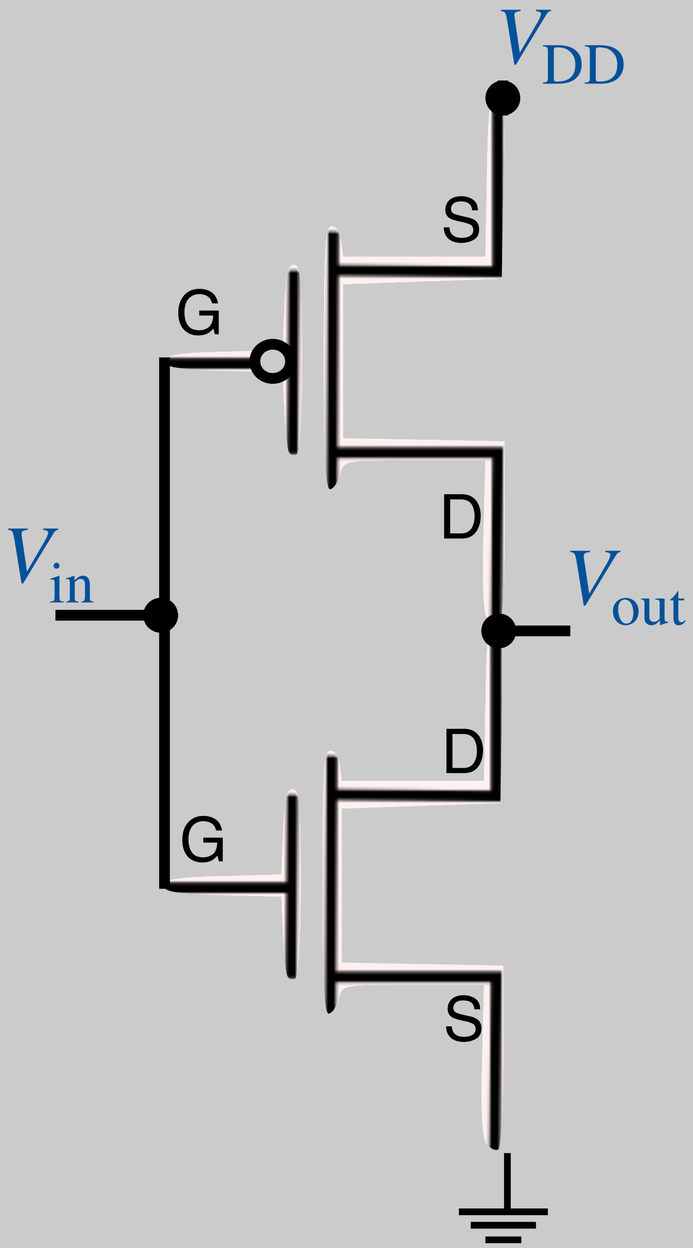


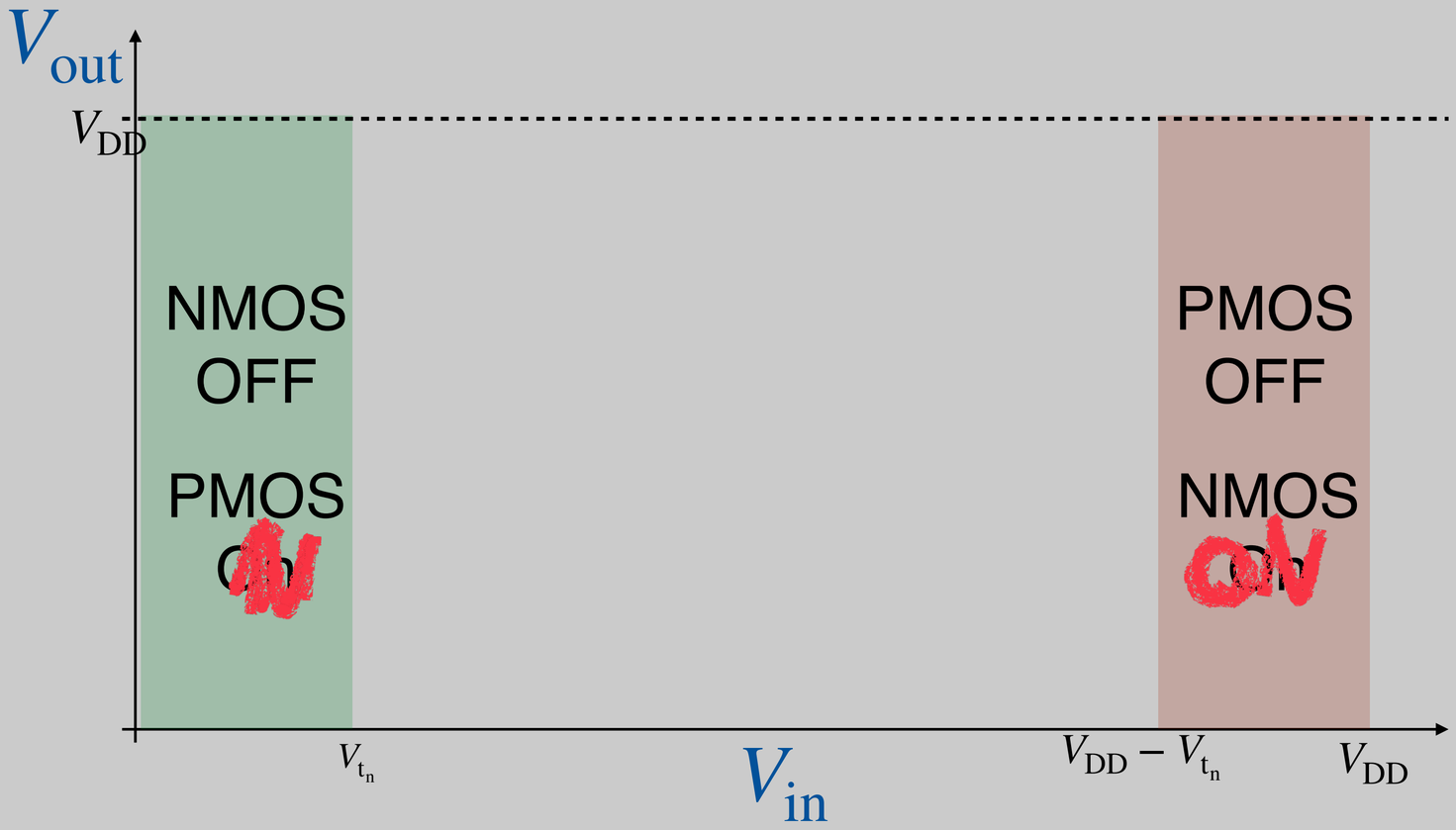
CMOS (Complementary MOS)



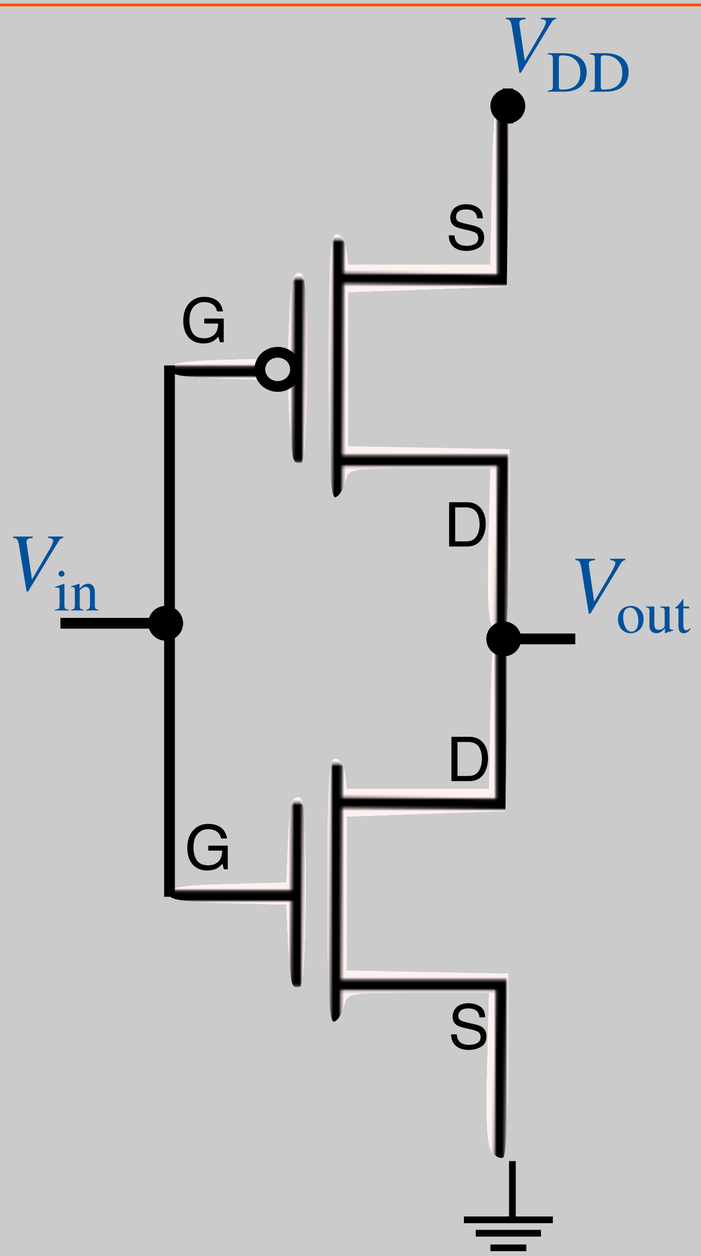


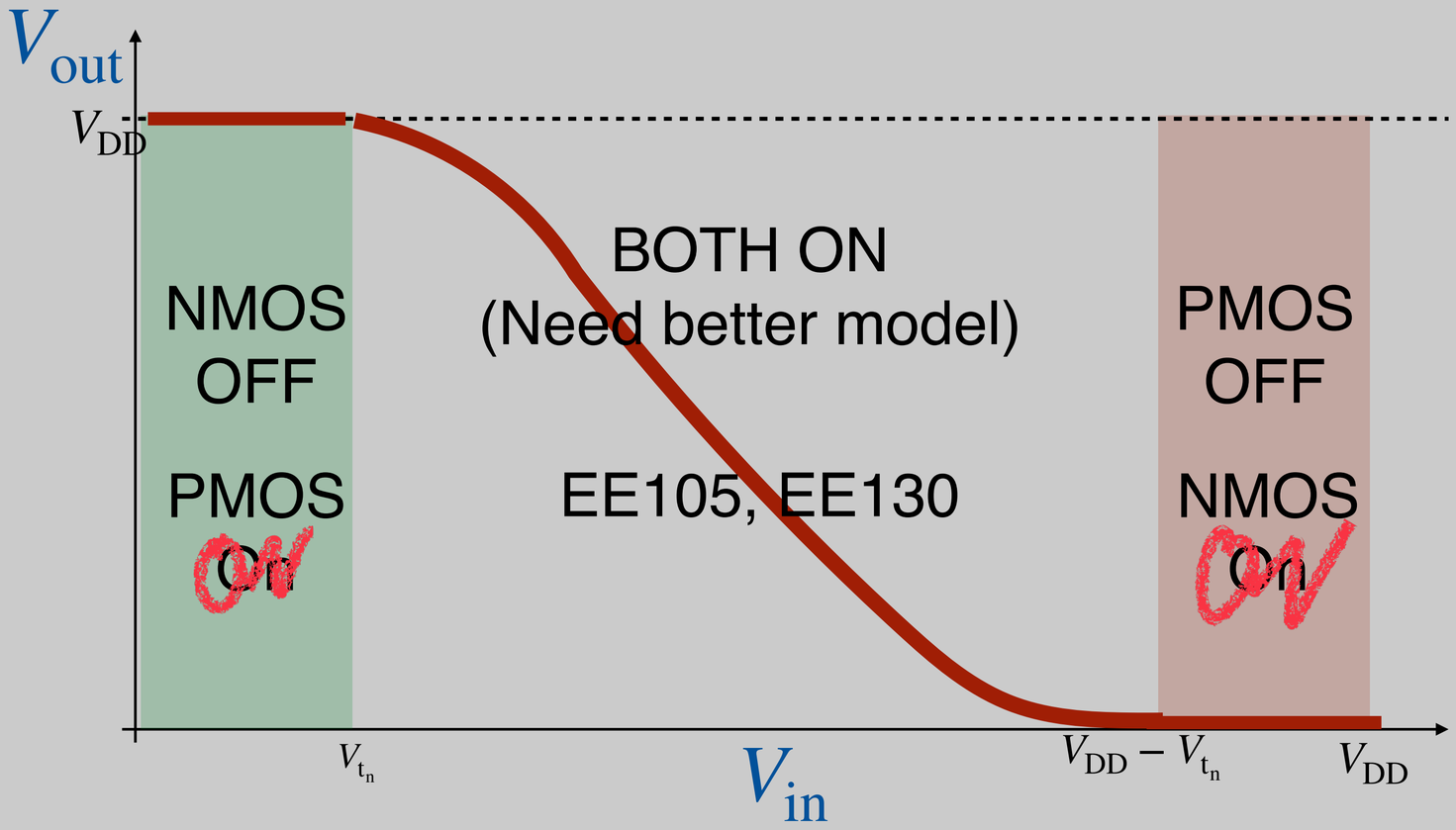
CMOS (Complementary MOS)



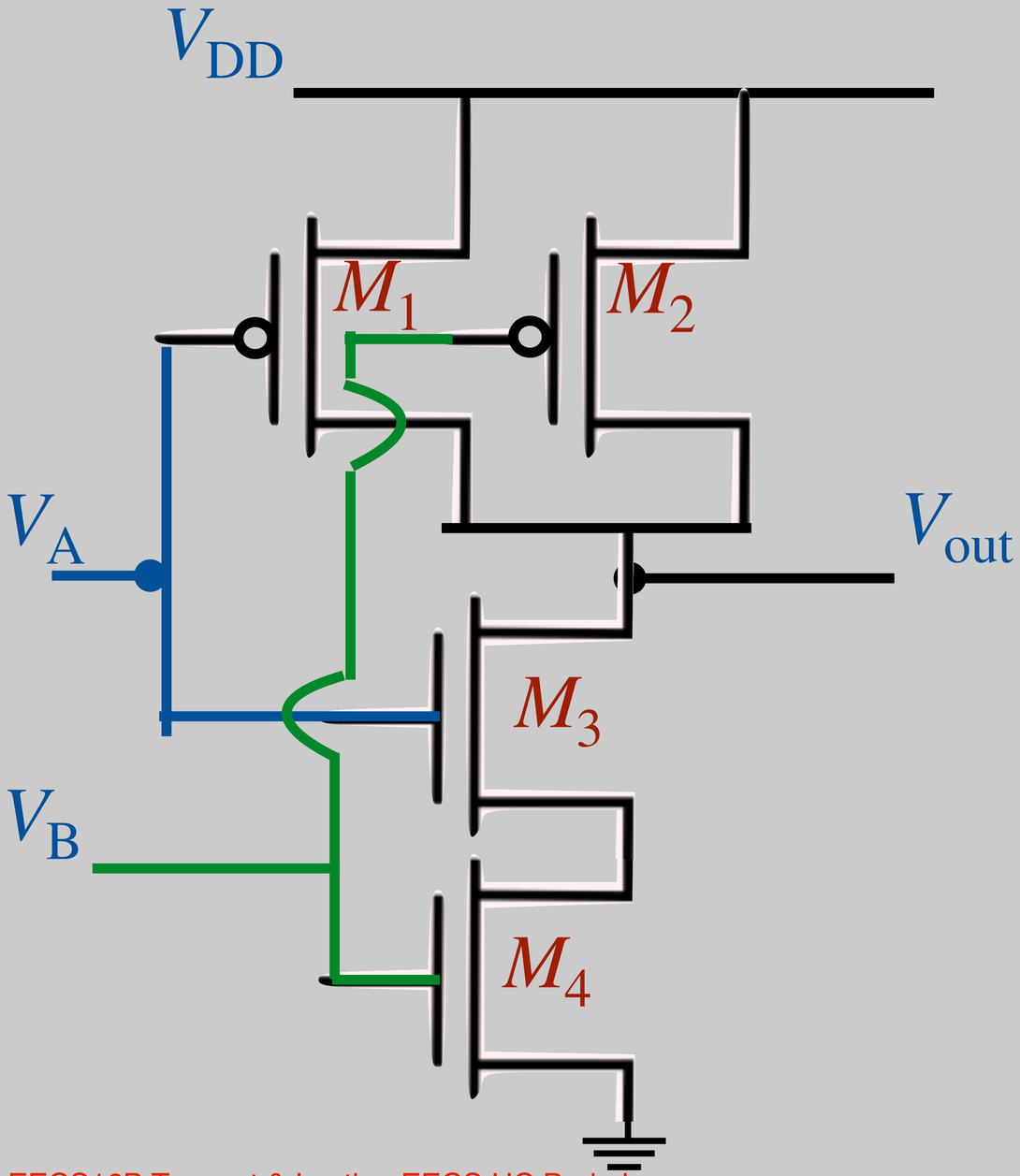


CMOS (Complementary MOS)



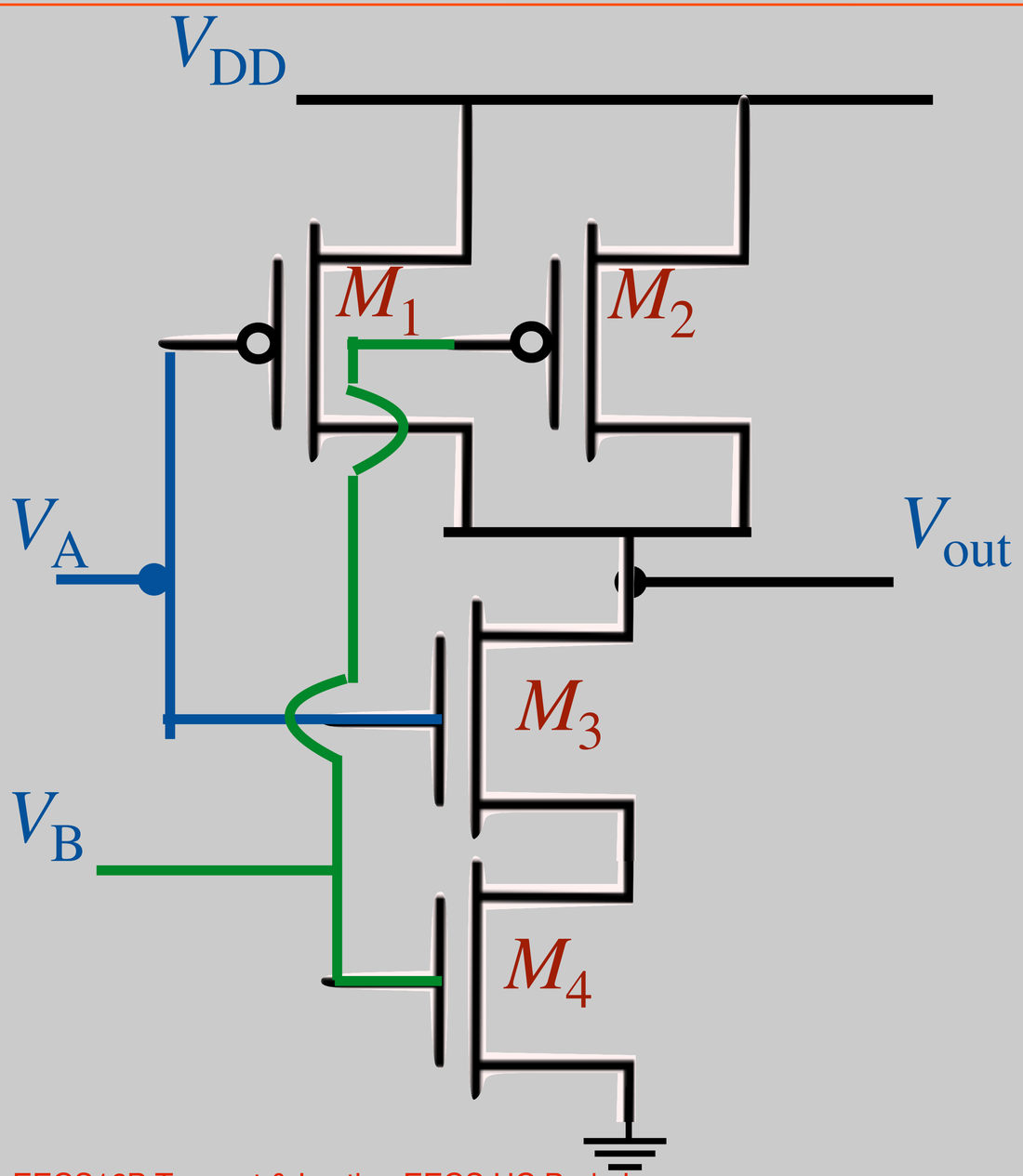


CMOS (Complementary MOS)



V_A	V_B	M_1	M_2	M_3	M_4	V_{out}
0	0					
0	1					
1	0					
1	1					

CMOS (Complementary MOS)



V_A	V_B	M_1	M_2	M_3	M_4	V_{out}
0	0	On	On	Off	Off	V_{DD}
0	1	On	Off	Off	On	V_{DD}
1	0	Off	On	On	Off	V_{DD}
1	1	Off	Off	On	On	0

NAND gate!