This homework is due on Saturday, February 10, 2024 at 11:59PM.

1. Transistor Logic Gates

(a) For this problem part, we will analyze the following transistor logic gate:

![CMOS logical circuit](image)

Assume that $V_{DD} = 1V$ and $V_{DD} > V_{Th}, |V_{Tp}| > 0$ (where $V_{Th}$ is the threshold voltage for the NMOS transistors and $V_{Tp}$ is the threshold voltage for the PMOS transistors) for all parts of the problem.

For each cell in the following table, for the given input voltages $V_A$ and $V_B$, fill in 1 for each transistor that is active (conducts current) for those input voltages and 0 otherwise. Then fill in the output voltage $V_{out}$, which should be either $V_{out} = V_{DD} = 1$ or $V_{out} = 0$. (Each element in the table should be either 0 or 1.) You may ignore the cell marked with an X.

You may model the transistors as voltage-controlled switches (with no resistance or capacitance).

<table>
<thead>
<tr>
<th>$V_A$</th>
<th>$V_B$</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
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<td></td>
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<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
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<td>X</td>
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<td>1</td>
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</tbody>
</table>

**Solution:** Transistors M1 and M2 are PMOS transistors. Transistors M3 and M4 are NMOS transistors. PMOS transistors are active/on (can be modelled as a closed switch) when $V_{SG} > |V_{Tp}|$ and NMOS transistors are active/on (can be modelled as a closed switch) when $V_{GS} > V_{Th}$. 
$V_{S,3}$ is the voltage of the source terminal of transistor M3, which is also the drain voltage for transistor M4; when transistor M4 is on, $V_{S,3} = 0$, but when M4 is off, $V_{S,3}$ is a disconnected node that can be between 0 and $V_{DD}$, which is why the case of $V_A = V_{DD}$ and $V_B = 0$ becomes more complicated (and was not asked).

For $V_A = V_B = 0$:
- $V_{SG,1} = V_{DD} - 0 = V_{DD} > |V_{TP}|$ so M1 is on.
- $V_{SG,2} = V_{DD} - 0 = V_{DD} > |V_{TP}|$ so M2 is on.
- $V_{GS,A} = 0 - 0 = 0 < V_{TN}$ so M4 is off.
- $V_{GS,3} = 0 - V_{S,3} < V_{TN}$ so M3 is off. $V_{S,3}$ is unknown, but $0 - V_{S,3} \leq 0$ since $0 \leq V_{S,3} \leq V_{DD}$.

Thus, $V_{out} = V_{DD}$ in this case since there is a conducting path from $V_{DD}$ to the output through both PMOS transistors (M1 and M2).

For $V_A = 0$ and $V_B = V_{DD}$:
- $V_{SG,1} = V_{DD} - V_{DD} = 0 < |V_{TP}|$ so M1 is off.
- $V_{SG,2} = V_{DD} - V_{DD} = 0 < |V_{TP}|$ so M2 is off.
- $V_{GS,A} = V_{DD} - 0 = V_{DD} > V_{TN}$ so M4 is on. This means that $V_{S,3} = 0$.
- $V_{GS,3} = 0 - V_{S,3} = 0 - 0 < V_{TN}$ so M3 is off.

Thus, $V_{out} = V_{DD}$ in this case since there is a conducting path from $V_{DD}$ to the output through PMOS transistor M1.

For $V_A = V_{DD}$ and $V_B = 0$:
- $V_{SG,1} = V_{DD} - V_{DD} = 0 < |V_{TP}|$ so M1 is off.
- $V_{SG,2} = V_{DD} - V_{DD} = 0 < |V_{TP}|$ so M2 is off.
- $V_{GS,A} = 0 - 0 = 0 < V_{TN}$ so M4 is off.
- This was the case where the state of transistor M3 was not asked.

Thus, $V_{out} = V_{DD}$ in this case since there is a conducting path from $V_{DD}$ to the output through PMOS transistor M2.

The state of transistor M3 does not matter in this case because transistor M4 being off means there cannot be a conductive path to ground and M2 being on means there is a conductive path to $V_{DD}$. In actuality, M3 would likely remain on until $V_{S,3} = V_{DD} - V_{TN}$ and would then turn off so in steady state, M3 would be off.

For $V_A = V_B = V_{DD}$:
- $V_{SG,1} = V_{DD} - V_{DD} = 0 < |V_{TP}|$ so M1 is off.
- $V_{SG,2} = V_{DD} - V_{DD} = 0 < |V_{TP}|$ so M2 is off.
- $V_{GS,A} = V_{DD} - 0 = V_{DD} > V_{TN}$ so M4 is on. This means that $V_{S,3} = 0$.
- $V_{GS,3} = V_{DD} - V_{DA} = V_{DD} - 0 = V_{DD} > V_{TN}$ so M3 is on.

Thus, $V_{out} = 0$ in this case since there is a conducting path from ground to the output through the combination of both NMOS transistors (M3 and M4).

The completed table would be the following. This is known as a NAND gate.
(b) For this problem part, we will analyze the following transistor logic gate:

![CMOS logical circuit](image)

The same assumptions hold as in the previous problem part. Fill in the following truth table with 1s and 0s. You may ignore the cell marked with an X.

<table>
<thead>
<tr>
<th>V_A</th>
<th>V_B</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>V_{out}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Solution:** With similar reasoning as the previous answer (except now the PMOS are in series and NMOS are in parallel), the completed table would be the following. This is known as a NOR gate.

<table>
<thead>
<tr>
<th>V_A</th>
<th>V_B</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>V_{out}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
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<td>1</td>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(c) Assume that you have access to three logic gates: the circuit from part (a) (Figure 1), the circuit from part (b) (Figure 2), and an inverter (Figure 3 below).
How could you construct an AND gate using these three logic gates? You may use as many or as few of each type of gate as you need. The truth table for an AND gate is as follows:

<table>
<thead>
<tr>
<th>$V_A$</th>
<th>$V_B$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Solution:** To make an AND gate, we can take the output of the NAND gate from part (a) and feed it into an inverter. This will flip all the $V_{out}$ values to match the given table.

(d) Once again assume you have access to the same three logic gates. How could you construct an OR gate? The truth table for an OR gate is as follows:

<table>
<thead>
<tr>
<th>$V_A$</th>
<th>$V_B$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Solution:** To make an OR gate, we can take the output of the NOR gate from part (b) and feed it into an inverter. This will flip all the $V_{out}$ values to match the given table.
2. Complex Algebra (Adapted from EE 120 Homework)

Consider the following two complex numbers throughout this problem:

\[ z_1 = 1 + j\sqrt{3} \]
\[ z_2 = e^{j\frac{2\pi}{3}} \]

(a) Plot each of the following complex numbers as points on the complex plane with a well-labeled sketch: \( z_1, z_2, z_1^*, z_2^*, \frac{1}{z_1}, \frac{1}{z_2} \).

**Solution:** See Figure 4 below.

![Figure 4: Complex numbers plotted on the complex plane.](image)

(b) Simplify the following expressions. You may express the answer as a real number, imaginary number, or complex number in Cartesian form or polar form.

i. \(|z_1z_2|\)

ii. \(|z_1z_2^*|\)

iii. \(z_1^3\)

iv. \(z_2^4\)

**Solution:**

i. \(|z_1z_2| = |z_1||z_2| = 2\)

ii. \(|z_1z_2^*| = |z_1||z_2^*| = |z_1||z_2| = 2\)

iii. \(z_1^3 = \left(2 \exp(j\frac{\pi}{3})\right)^3 = 8 \exp(j\pi) = -8\)

iv. \(z_2^4 = \left(\exp(j\frac{2\pi}{3})\right)^4 = \exp(j\frac{8\pi}{3}) = \exp(j\frac{2\pi}{3}) = z_2\)
(c) Determine $z^{1/4}_2$. Note that $z_2$ may have multiple fourth roots. Express your answer(s) in polar form.

Solution:

$$z^{1/4}_2 = \exp\left( j\left(2n\pi + \frac{2\pi}{3}\right)\right)^{1/4} \forall n \in \{0, 1, 2, 3\}$$

$$= \exp\left(j \left(\frac{2\pi}{3}\right)\right)^{1/4}, \exp\left(j \left(2\pi + \frac{2\pi}{3}\right)\right)^{1/4}, \exp\left(j \left(4\pi + \frac{2\pi}{3}\right)\right)^{1/4}$$

$$= \exp\left(j \frac{\pi}{6}\right), \exp\left(j \left(\frac{\pi}{2} + \frac{\pi}{6}\right)\right), \exp\left(j \left(\frac{\pi}{2} + \frac{\pi}{6}\right)\right), \exp\left(j \left(\frac{3\pi}{2} + \frac{\pi}{6}\right)\right)$$

$$= \exp\left(j \frac{\pi}{6}\right), \exp\left(j \frac{2\pi}{3}\right), \exp\left(j \frac{7\pi}{6}\right), \exp\left(j \frac{5\pi}{3}\right)$$
3. RLC Circuit 1

A DC source is connected to a series RLC circuit by a switch that closes at \( t = 0 \), as shown in Figure 5. The initial conditions are \( i(0+) = 0 \) and \( v_C(0+) = 25 \). Write the differential equation for \( v_C(t) \). Solve for \( v_C(t) \) given that \( R = 80 \, \Omega \).

![Circuit diagram.](image)

**Solution:** We can apply KVL to the circuit to obtain:

\[
50 = v_L(t) + v_R(t) + v_C(t) \\
= L \frac{di(t)}{dt} + i(t)R + v_C(t) \\
= L \frac{di(t)}{dt} + RC \frac{dv_C(t)}{dt} + v_C(t)
\]

Now, we have that \( L \frac{di(t)}{dt} = L \frac{d}{dt} \left( C \frac{dv_C(t)}{dt} \right) = LC \frac{d^2v_C(t)}{dt^2} \). Plugging this in, we get

\[
LC \frac{d^2v_C(t)}{dt^2} + RC \frac{dv_C(t)}{dt} + v_C(t) = 50
\]

(4)

\[
\frac{d^2v_C(t)}{dt^2} + \frac{R}{L} \frac{dv_C(t)}{dt} + \frac{1}{LC} v_C(t) = \frac{50}{LC}
\]

(5)

We have a second order differential equation, so our solution will be of the form \( v_C(t) = v_{C_p}(t) + v_{C_h}(t) \), where \( v_{C_p}(t) \) is the particular solution and \( v_{C_h}(t) \) is the homogeneous solution. Here, we have a DC forcing function (i.e., \( f(t) = \frac{50}{LC} \)). Hence, the particular solution would be the solution if we replaced inductors with short circuits and capacitances with open circuits. This yields \( v_{C_p}(t) = 50 \).

To find \( \alpha \) and \( \omega_0 \), we can pattern match \( \omega_0 = \sqrt{\frac{1}{LC}} = 10^4 \) and \( 2\alpha = \frac{R}{L} \Rightarrow \alpha = \frac{R}{2L} = 2 \times 10^4 \) from Note 5. Since \( \alpha > \omega_0 \), the homogeneous solution will be of the form

\[
v_{C_h}(t) = K_1 e^{\alpha t} + K_2 e^{\omega t}
\]

(6)

where \( s_1 = -\alpha + \sqrt{\alpha^2 - \omega^2} = -2679.49 \) and \( s_2 = -\alpha - \sqrt{\alpha^2 - \omega^2} = -37320.5 \). Hence, the final solution is of the form

\[
v_C(t) = v_{C_p}(t) + v_{C_h}(t) = 50 + K_1 e^{\alpha t} + K_2 e^{\omega t}
\]

(7)

To find \( K_1 \) and \( K_2 \), we can utilize the fact that \( v_C(0) = 25 \) and \( \frac{dv_C(t)}{dt}|_{t=0} = \frac{i(0)}{C} = 0 \). Plugging these in, we get the following system:

\[
v_C(0) = 25 = 50 + K_1 + K_2
\]

(8)
\[ \frac{dv_C(t)}{dt} \bigg|_{t=0} = 0 = s_1 K_1 + s_2 K_2 \quad (9) \]

Solving this system of equation yields \( K_1 = -26.93 \) and \( K_2 = 1.93 \). Hence, the final answer is

\[ v_C(t) = 50 + (-26.93)e^{-2679.49t} + (1.93)e^{-37320.5t} \quad (10) \]
4. RLC Circuit 2

Consider the circuit shown in Figure 6, with $R = 25\, \Omega$.

![Figure 6: Circuit diagram.](image)

(a) Compute the undamped resonant frequency, $\omega_0$, and $\alpha$.

**Solution:** From KCL, we have

$$1 = i_R(t) + i_L(t) + i_C(t) \quad (11)$$

$$= \frac{v(t)}{R} + i_L(t) + C \frac{dv(t)}{dt} \quad (12)$$

Taking derivatives on both sides, we get

$$C \frac{d^2v(t)}{dt^2} + \frac{1}{R} \frac{dv(t)}{dt} + \frac{1}{L} v(t) = 0 \quad (13)$$

We also know that $v(t) = L \frac{di_L(t)}{dt}$. Plugging this in, we get

$$C \frac{d^2v(t)}{dt^2} + \frac{1}{R} \frac{dv(t)}{dt} + \frac{1}{L} v(t) = 0 \quad (14)$$

$$\frac{d^2v(t)}{dt^2} + \frac{1}{RC} \frac{dv(t)}{dt} + \frac{1}{LC} v(t) = 0 \quad (15)$$

Pattern matching to Note 5, we get $\omega_0 = \sqrt{\frac{1}{LC}} = 1 \times 10^7$ and $2\alpha = \frac{1}{RC} = 4 \times 10^7 \implies \alpha = 2 \times 10^7$. Hence, it is an overdamped circuit ($\alpha > \omega_0$).

(b) The initial conditions are $v(0+) = 0$ and $i_L(0+) = 0$. Show that this requires $v'(0+) = 10^9 \frac{V}{s}$.

**Solution:** We still must satisfy KCL at $t = 0+$, so we have

$$1 = i_R(0+) + i_L(0+) + i_C(0+) \quad (16)$$

$$= \frac{v(0+)}{R} + i_L(0+) + C v'(0+) \quad (17)$$

$$= C v'(0+) \quad (18)$$

This leaves us with $v'(0+) = \frac{1}{C} = 10^9 \frac{V}{s}$.

(c) Find the particular solution for $v(t)$.

**Solution:** To find the particular solution, we first notice that the forcing function is $f(t) = 0$ which is a constant. Hence, we can replace capacitors with open circuits and inductors with short circuits. If we were to do this, all of the current flows through the branch with the inductor and the particular solution is $v_p(t) = 0$. 
(d) Find the general solution for $v(t)$, including the numerical values of all parameters.

**Solution:** Since $\alpha > \omega_0$, the homogeneous solution will be of the form

$$v_C(t) = K_1e^{s_1t} + K_2e^{s_2t} \quad (19)$$

where $s_1 = -\alpha + \sqrt{\alpha^2 - \omega_0^2} = -2.68 \times 10^6$ and $s_2 = -\alpha - \sqrt{\alpha^2 - \omega_0^2} = -3.73 \times 10^7$. Since the particular solution $v_p(t) = 0$, we have that

$$v(t) = K_1e^{s_1t} + K_2e^{s_2t} \quad (20)$$

Now, we will use our initial conditions of $v(0) = 0$ and $v'(0) = 10^9$. Plugging these in, we get the following system of equations:

$$v(0) = 0 = K_1 + K_2 \quad (21)$$
$$v'(0) = 10^9 = s_1K_1 + s_2K_2 \quad (22)$$

Solving the system of equations yields $K_1 = 28.89$ and $K_2 = -28.89$. Thus, the final answer is

$$v(t) = 28.89e^{(-2.68 \times 10^6)t} - 28.89e^{(-3.73 \times 10^7)t} \quad (23)$$

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