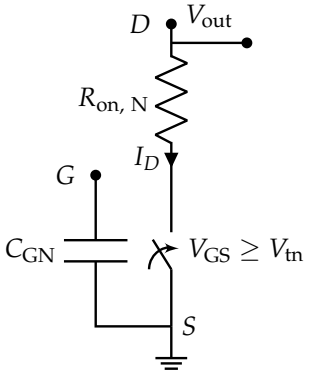
Discussion 5B

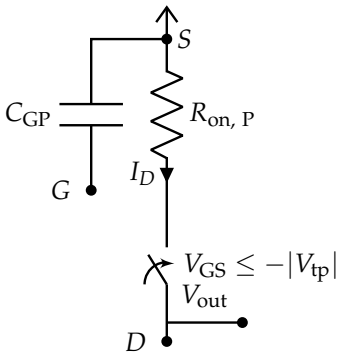
This discussion is a continuation of Discussion 5A.

1. Transistor Switch Model

(Repeated from Discussion 5A) As seen in lecture, we can model the behavior of a transistor with a capacitor and resistor. In this model, the gate capacitances C_{GN} and C_{GP} represent the lumped physical capacitance present on the gate node of all transistor devices. This capacitance is important as it determines the delay of a transistor logic chain.



(a) NMOS Resistor-switch-capacitor model



(b) PMOS Resistor-switch-capacitor model

In the configuration below, you have two CMOS inverters made from NMOS and PMOS devices. The two inverters are connected in series, with the output of the first inverter driving the input of the second inverter (Figure 2).

Both NMOS and PMOS devices have an "on resistance" of $R_{on,\,N} = R_{on,\,P} = 1\ \text{k}\Omega$, and each has a gate capacitance (input capacitance) of $C_{GN} = C_{GP} = 1\ \text{fF}$ (fF = femto-Farads = 1×10^{-15} F).

We assume the "off resistance" (the resistance when the transistor is off) is infinite (i.e., the transistor acts as an open circuit when off). The supply voltage V_{DD} is 1V.

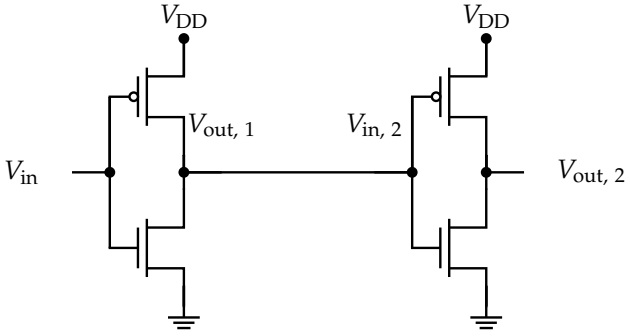


Figure 2: CMOS Inverter chain

(a) Recall that in the previous discussion, we derived that the RC circuit for the output of the first inverter was:

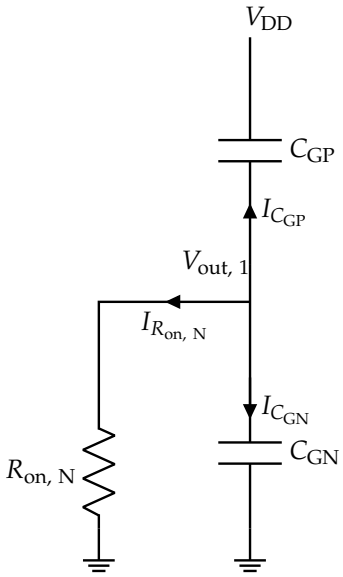


Figure 3: First inverter output at 0

The corresponding differential equation for the output of the first inverter was

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{\text{out},\,1}(t) = -\frac{V_{\text{out},\,1}(t)}{R_{\text{on, N}}(C_{\text{GP}} + C_{\text{GN}})} \tag{1}$$

This was assumimg that the input to the first inverter has been low ($V_{\text{in}} = 0$ V) for a long time, and then switches at time $t = 0$ to high ($V_{\text{in}} = V_{\text{DD}}$).

Using these initial conditions, **solve for** $V_{\text{out},\,1}(t)$**.**

Solution: We know that the solution to a differential equation of the form

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{\text{out},\,1}(t) = -\frac{V_{\text{out},\,1}}{R_{\text{on, N}}(C_{\text{GP}} + C_{\text{GN}})} \tag{2}$$

is

$$V_{\text{out},\,1}(t) = k\mathrm{e}^{-\frac{t}{R_{\text{on, N}}(C_{\text{GP}}+C_{\text{GN}})}} \tag{3}$$

Plugging in the initial condition $V_{\text{out},\,1}(0) = V_{\text{DD}}$ we find that $V_{\text{out},\,1}(t) = V_{\text{DD}}\mathrm{e}^{-\frac{t}{R_{\text{on, N}}(C_{\text{GP}}+C_{\text{GN}})}}$.

(b) **Sketch the output voltage of the first inverter, showing clearly (1) the initial value, (2) the initial slope, (3) the asymptotic value, and (4) the time that it takes for the voltage to decay to roughly 1/3 of its initial value.**

Solution:

(1) We know that the output of our inverter started with the initial value V_{DD}.

(2) Since the differential equation tells us the change in value of $V_{\text{out},\,1}(t)$ at time t we can simply plug in $t = 0$ into our differential equation to get the initial slope:

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{\text{out},\,1}(t) = -\frac{V_{\text{out},\,1}(0)}{R_{\text{on, N}}(C_{\text{GP}} + C_{\text{GN}})} \tag{4}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}V_{\text{out, 1}}(t) = -\frac{V_{\text{DD}}}{R_{\text{on, N}}(C_{\text{GP}} + C_{\text{GN}})} \tag{5}$$

Thus the initial slope is $-\frac{V_{\text{DD}}}{R_{\text{on, N}}(C_{\text{GP}}+C_{\text{GN}})}$.

(3) Since the input to the inverter changed from low to high we know the output of the first inverter ($V_{\text{out, 1}}$) is going to go to 0 in steady state, as this node will be discharged by the first inverter's NMOS transistor.
Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{\text{out, 1}}(t)$ to find $V_{\text{out, 1}} = V_{\text{DD}}\mathrm{e}^{-\frac{\infty}{R_{\text{on, N}}(C_{\text{GP}}+C_{\text{GN}})}} = 0$.

(4) To approximate when the output will decay to $\frac{1}{3}$ its original value, we use the fact that $\mathrm{e}^{-1} = \frac{1}{e} \approx \frac{1}{3}$. We thus want to find when $V_{\text{out, 1}} = V_{\text{DD}}\mathrm{e}^{-1}$.
This will occur when the e term is raised to -1, which occurs when $t = R_{\text{on, N}}(C_{\text{GP}} + C_{\text{GN}}) = 2 \times 10^{-12}$s.
You should also give yourself full credit if you used $\frac{1}{3}$ itself and computed $-\ln(3)$, etc.

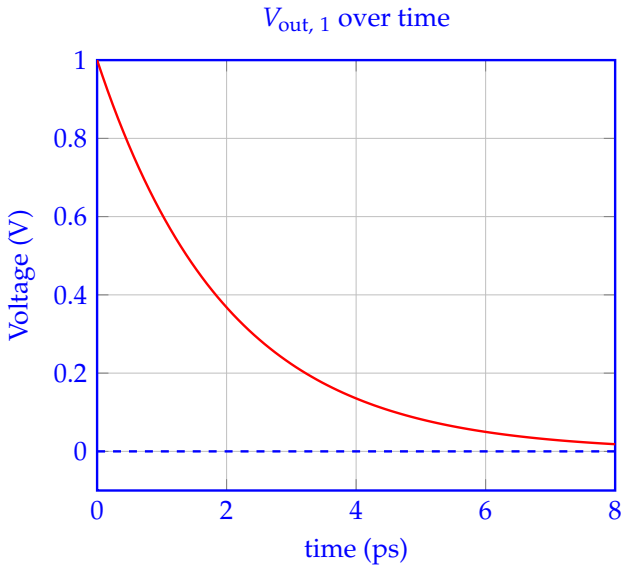


Figure 4

(c) A long time later, the input to the first inverter switches low again.

Draw the new RC circuit and set up another differential equation for $V_{\text{out, 1}}(t)$. *(HINT: This should look very similar to what we solved for Discussion 5A. What is different about our circuit?)*

Solution: We know that after a long time, the output of the first inverter has stabilized to 0. When the input switches low again, the input inverter's NMOS device turns off, while the input inverter's PMOS device turns on. This connects the $V_{\text{out, 1}}$ node to V_{DD}, as shown in Figure 5.

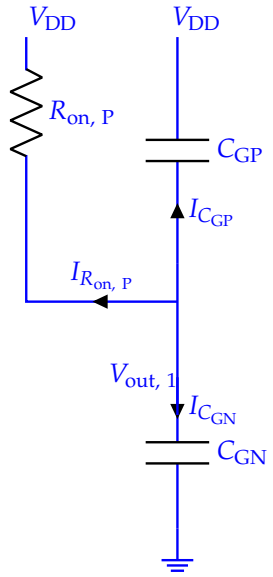


Figure 5: Inverter output at 1

To set up the differential equation, we apply KVL and KCL again:

$$I_{C_{GP}} = C_{GP}\frac{d}{dt}(V_{out,\,1}(t) - V_{DD}) \tag{6}$$

$$I_{C_{GN}} = C_{GN}\frac{d}{dt}V_{out,\,1}(t) \tag{7}$$

$$I_{R_{on,\,P}} = \frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{8}$$

$$I_{C_{GP}} + I_{C_{GN}} = -I_{R_{on,\,P}} \tag{9}$$

$$C_{GP}\frac{d}{dt}(V_{out,\,1}(t) - V_{DD}) + C_{GN}\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{10}$$

$$C_{GP}\frac{d}{dt}V_{out,\,1}(t) + C_{GN}\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{11}$$

$$(C_{GP} + C_{GN})\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}} \tag{12}$$

$$\frac{d}{dt}V_{out,\,1}(t) = -\frac{V_{out,\,1}(t) - V_{DD}}{R_{on,\,P}(C_{GP} + C_{GN})} \tag{13}$$

(d) **Solve for $V_{out,\,1}(t)$.**

Solution: Rewriting the differential equation into standard form yields:

$$\frac{d}{dt}V_{out,\,1}(t) + \frac{1}{R_{on,\,P}(C_{GP} + C_{GN})}V_{out,\,1}(t) = \frac{V_{DD}}{R_{on,\,P}(C_{GP} + C_{GN})} \tag{14}$$

From here, we recognize that we have a first order non-homogeneous differential equation, which we can use a variety of techniques to solve such as the integrating factor method, pattern matching, or using the general solution to a first order differential equation (we will use this method).

Recall, the general solution is:

$$y(t) = Ae^{-at} + e^{-at}\int e^{at'}b(t')\,dt' \tag{15}$$

For simplicity let's substitute $\tau = R_{\text{on, P}}(C_{\text{GP}} + C_{\text{GN}})$. Plugging in our values for a and $b(t)$ and solving, we get:

$$V_{\text{out, 1}}(t) = Ae^{-\frac{1}{\tau}t} + e^{-\frac{1}{\tau}t}\int_0^t e^{\frac{1}{\tau}t'}\frac{V_{\text{DD}}}{\tau}\,dt' \tag{16}$$

$$V_{\text{out, 1}}(t) = Ae^{-\frac{1}{\tau}t} - \frac{V_{\text{DD}}}{\tau}e^{-\frac{1}{\tau}t}\int_0^t e^{\frac{1}{\tau}t'}\,dt' \tag{17}$$

$$V_{\text{out, 1}}(t) = Ae^{-\frac{1}{\tau}t} + \frac{V_{\text{DD}}}{\tau}e^{-\frac{1}{\tau}t}\left(\tau e^{\frac{1}{\tau}t'}\right)_0^t \tag{18}$$

$$V_{\text{out, 1}}(t) = Ae^{-\frac{1}{\tau}t} + V_{\text{DD}}e^{-\frac{1}{\tau}t}\left[e^{\frac{1}{\tau}t} - 1\right] \tag{19}$$

$$V_{\text{out, 1}}(t) = Ae^{-\frac{1}{\tau}t} + V_{\text{DD}}\left(1 - e^{-\frac{1}{\tau}t}\right) \tag{20}$$

Substituting $\tau = R_{\text{on, P}}(C_{\text{GP}} + C_{\text{GN}})$ back in, we get

$$V_{\text{out, 1}}(t) = V_{\text{DD}} + (A - V_{\text{DD}})e^{-\frac{t}{R_{\text{on, P}}(C_{\text{GP}}+C_{\text{GN}})}} \tag{21}$$

Using the initial condition $V_{\text{out, 1}} = 0$ (as the input to the first inverter was high for a long time before switching low) implies $A = 0$. Thus:

$$V_{\text{out, 1}}(t) = V_{\text{DD}}\left(1 - e^{-\frac{t}{R_{\text{on, P}}(C_{\text{GP}}+C_{\text{GN}})}}\right) \tag{22}$$

(e) **(PRACTICE) Sketch the output voltage of the first inverter ($V_{\text{out, 1}}$), showing clearly (1) the initial value, (2) the initial slope, and (3) the asymptotic value.**

Solution:

(1) Because the input to the first inverter was high for a long time, we know the initial value of $V_{\text{out, 1}}(t) = 0$. This was the initial condition applied to the solution of the differential equation, above.

(2) To find the initial value of the slope we can plug in $t = 0$ to the above differential equation:

$$\frac{d}{dt}V_{\text{out, 1}}(t) = \frac{(V_{\text{DD}} - V_{\text{out, 1}}(0))}{R_{\text{on, P}}(C_{\text{GP}} + C_{\text{GN}})} \tag{23}$$

where $V_{\text{out, 1}}(0) = 0$. Thus our initial slope is $\frac{(V_{\text{DD}})}{R_{\text{on, P}}(C_{\text{GP}}+C_{\text{GN}})}$. Notice this slope is positive while the previous part had a negative slope.

(3) Since the input to the inverter changed from low to high and the input inverter's PMOS is now on, we know the output of the first inverter is going to go to V_{DD} in steady state.

(4) Alternatively, we can find the asymptotic value by plugging in $t = \infty$ to the solution we found for $V_{\text{out, 1}}(t)$ to find $V_{\text{out, 1}} = V_{\text{DD}}\left(1 - e^{-\frac{\infty}{R_{\text{on, P}}(C_{\text{GP}}+C_{\text{GN}})}}\right) = V_{\text{DD}}(1 - 0) = V_{\text{DD}}$.

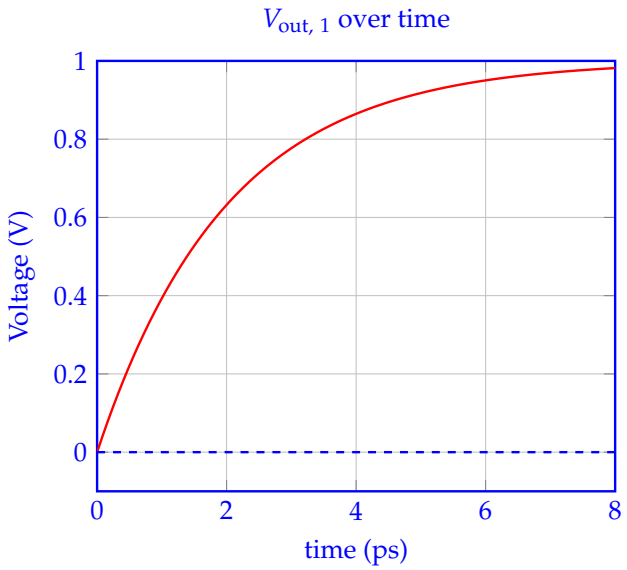


Figure 6

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