This discussion relies on material covered in lecture on transistors (01/25).

1. Transistor Switch Model (Adapted from Spring 2021 Midterm 1)

In this problem, we will analyze the behavior of a NAND gate driving an inverter. 1a shows the transistor model of a NAND gate and 1b shows the transistor model of an inverter.

In this question assume that $V_{DD}$ is greater than both the NMOS threshold $V_{th,n}$ and PMOS threshold $|V_{th,p}|$.

(a) A diagram of a NAND gate driving an inverter is shown in 2a. Consider the case where $A = V_{DD}$ and $B = V_{DD}$ for a long time before $t = 0$. Then at $t = 0$, we switch $A$ and $B$ to 0V. The equivalent simplified circuit after this transition is shown in 2b. Find $V_{out}$ at time $t = 0$.

**Solution:** $V_{out}(0) = 0$. Since $A = B = V_{DD}$ for $t < 0$, both NMOS transistors have been switched on due to $V_{GSn} = V_{DD} > V_{th,n}$ until right before $t = 0$.

Similarly, both PMOS transistors are switched off because $|V_{GSp}| = 0 \leq |V_{th,p}|$. Therefore, $C_{N,INV}$ is fully discharged to 0V and $C_{P,INV}$ is fully charged to $V_{DD}$ right before $t = 0$. When the transition happens the charge on capacitors cannot jump instantaneously. So, at $t = 0$ the voltage at output will remain 0V.

(b) Write the differential equation for solving $V_{out}(t)$ for $t \geq 0$ in the circuit shown in 2b. Specifically, find coefficients $\lambda$ and $b$ in the following symbolic differential equation:

$$\frac{dV_{out}(t)}{dt} = \lambda V_{out}(t) + bV_{DD},$$  \hspace{1cm} (1)
Figure 2: Schematic and model of a NAND gate driving an inverter

as a function of $R_P, C_{P,\text{INV}}, C_{N,\text{INV}},$ and $V_{DD}$. Assume that $R_{P,\text{NAND}} = R_{P,\text{NAND}} = R_P$.

**Solution:** The first thing to note is that the two resistors are in parallel, so we can lump them into one resistor with half the value. We can then start by writing a KCL at the output node:

$$C_{N,\text{INV}} \frac{dV_{out}(t)}{dt} + C_{P,\text{INV}} \frac{d(V_{out}(t) - V_{DD})}{dt} + \frac{2}{R_P} (V_{out}(t) - V_{DD}) = 0,$$

$$\frac{dV_{out}(t)}{dt} = -\frac{2}{R_P(C_{P,\text{INV}} + C_{N,\text{INV}})} V_{out}(t) + \frac{2}{R_P(C_{P,\text{INV}} + C_{N,\text{INV}})} V_{DD}.$$ 

Therefore, $\lambda = -\frac{2}{R_P(C_{P,\text{INV}} + C_{N,\text{INV}})}$ and $b = \frac{2}{R_P(C_{P,\text{INV}} + C_{N,\text{INV}})}$.

(c) **Solve the differential equation for $V_{out}(t)$**. You should leave your answer in terms of $\lambda, b, V_{DD}$, and $V_{out}(0)$.

**Solution:** Recall that solving a circuit differential equation has four key steps.

i. Use node voltage analysis and circuit analysis methods to set up a differential equation.

ii. Solve for the homogeneous solution

iii. Solve for the particular solution using the steady-state value.

iv. Combine your homogeneous and particular solutions, and solve for the unknown coefficient using your initial condition.

We’ve already completed step 1. Let us complete the remaining steps.

**Homogeneous Solution:** We know that our homogenous solution solves the following differential equation:

$$\frac{dV_{out}(t)}{dt} = \lambda V_{out}(t)$$

(2)

From lecture and notes we know that the solution to this equation is given as:

$$V_{out, h}(t) = Ae^{\lambda t}$$

(3)

**Particular Solution:** In steady-state, we know that capacitors are equivalent to open circuits. But wait, with $C_{P,\text{INV}}$ and $C_{P,\text{INV}}$ being open circuits, there is no current flow in the remaining circuit. Therefore, our particular solution is simply given as:
\[ V_{\text{out}, p}(t) = V_{\text{out}}(t) = V_{DD} \]  

**Solving for Coefficient Using Initial Condition:** From part (a), we know that our initial solution is given by \( V_{\text{out}}(0) = 0 \text{volt} \). Thus, we solve for \( A \) as follows:

\[ V_{\text{out}}(0) = V_{\text{out}, h}(0) + V_{\text{out}, p}(0) \]  

\[ Ae^{\lambda t} + V_{DD} = 0 \]  

\[ A = -V_{DD} \]

Thus, our final solution is:

\[ V_{\text{out}}(t) = V_{DD}(1 - e^{\lambda t}) \]

(d) Now consider the case where \( A = 0 \text{V} \) and \( B = 0 \text{V} \) for a long time before \( t = 0 \) in 2a. At \( t = 0 \) we switch \( A \) and \( B \) to \( V_{DD} \). Write down the state (ON/OFF) of transistors P1, P2, N1, and N2 in the NAND gate. Draw the equivalent simplified circuit for this transition that will help us with writing the differential equation of \( V_{\text{out}}(t) \).

*(HINT: You may find the NAND resistor-switch model in 3 helpful. Don’t forget to include the inverter’s capacitors, \( C_{N, \text{INV}} \) and \( C_{P, \text{INV}} \), which are loading the NAND gate.)*
Figure 3: NAND Model: Capacitances

Solution: Both of our inputs are high ($V_{DD}$). Thus $|V_{GSP}| = 0V \implies$ both PMOS transistors P1 and P2 are OFF. At the same time $V_{GSn} = V_{DD} \implies$ both NMOS transistors N1 and N2 are ON. Since the PMOS transistors are both off, their switches in the equivalent circuit are open. As a result their resistors $R_{P1,NAND}$ and $R_{P2,NAND}$ are floating and don’t need to be included.

The NMOS transistors, on the other hand, are both on, so in the simplified equivalent circuit, their resistors $R_{N1,NAND}$ and $R_{N2,NAND}$ connect the output to ground.

In addition, $V_{out}$ drives an inverter, which means that $V_{out}$ is connected to two gate capacitances: $C_{P,INV}$ to $V_{DD}$ and $C_{N,INV}$ to ground.

Thus we end up with the simplified circuit below.

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\[ V_{DD} \]

\[ C_{P, \text{INV}} \]

\[ V_{out(t)} \]

\[ R_{N1, \text{NAND}} \]

\[ C_{N, \text{INV}} \]

\[ R_{N2, \text{NAND}} \]