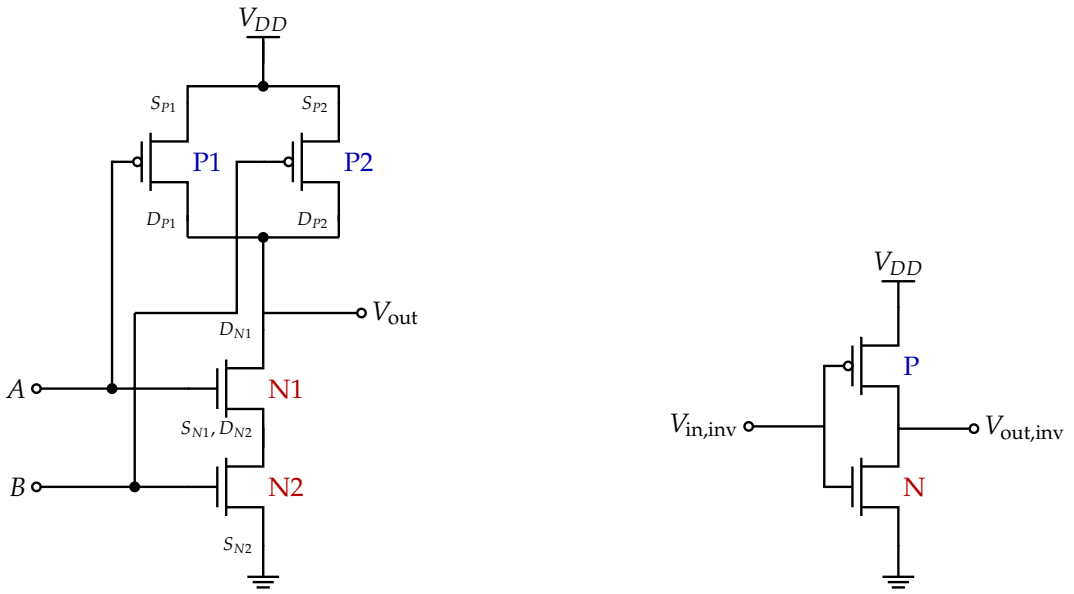
Discussion 3B

This discussion relies on material covered in lecture on transistors (**01/25**).

1. Transistor Switch Model (Adapted from Spring 2021 Midterm 1)

In this problem, we will analyze the behavior of a NAND gate driving an inverter. 1a shows the transistor model of a NAND gate and 1b shows the transistor model of an inverter.

In this question assume that V_{DD} is greater than both the NMOS threshold $V_{\text{th,n}}$ and PMOS threshold $|V_{\text{th,p}}|$.

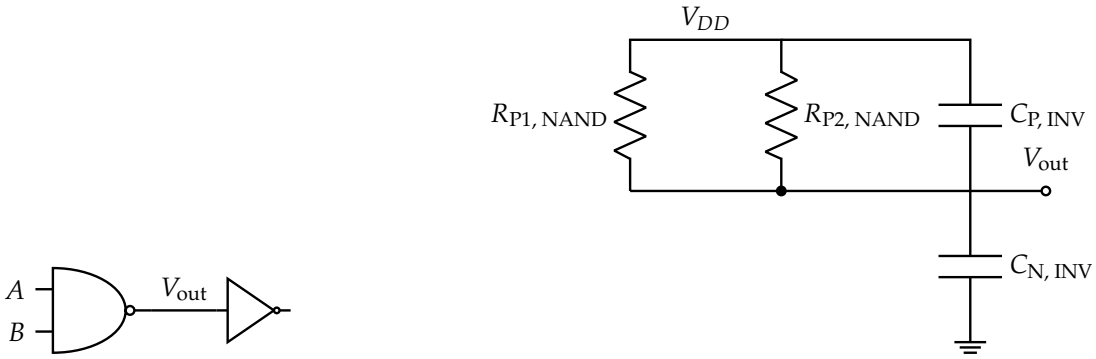


(a) NAND schematic with transistors.

(b) Inverter schematic with transistors.

Figure 1: Transistor schematics

(a) A diagram of a NAND gate driving an inverter is shown in 2a. Consider the case where $A = V_{DD}$ and $B = V_{DD}$ for a long time before $t = 0$. Then at $t = 0$, we switch A and B to 0V. The equivalent simplified circuit after this transition is shown in 2b. **Find** V_{out} **at time** $t = 0$.



(a) NAND driving an Inverter

(b) A Simplified Equivalent Circuit for when $A = B = 0$V

Figure 2: Schematic and model of a NAND gate driving an inverter

(b) **Write the differential equation for solving $V_{\text{out}}(t)$ for $t \geq 0$ in the circuit shown in 2b**. Specifically, **find coefficients λ and b in the following symbolic differential equation:**

$$\frac{dV_{\text{out}}(t)}{dt} = \lambda V_{\text{out}}(t) + bV_{DD}, \tag{1}$$

as a function of R_P, $C_{\text{P, INV}}$, $C_{\text{N, INV}}$, and V_{DD}. Assume that $R_{\text{P1,NAND}} = R_{\text{P2, NAND}} = R_P$.

(c) **Solve the differential equation for $V_{\text{out}}(t)$**. You should leave your answer in terms of λ, b, V_{DD}, and $V_{\text{out}}(0)$.

(d) Now consider the case where $A = 0\text{V}$ and $B = 0\text{V}$ for a long time before $t = 0$ in 2a. At $t = 0$ we switch A and B to V_{DD}. **Write down the state (ON/OFF) of transistors P1, P2, N1, and N2 in the NAND gate. Draw the equivalent simplified circuit for this transition that will help us with writing the differential equation of $V_{\text{out}}(t)$.**

(HINT: You may find the NAND resistor-switch model in 3 helpful. Don't forget to include the inverter's capacitors, $C_{N,\,INV}$ and $C_{P,\,INV}$, which are loading the NAND gate.)

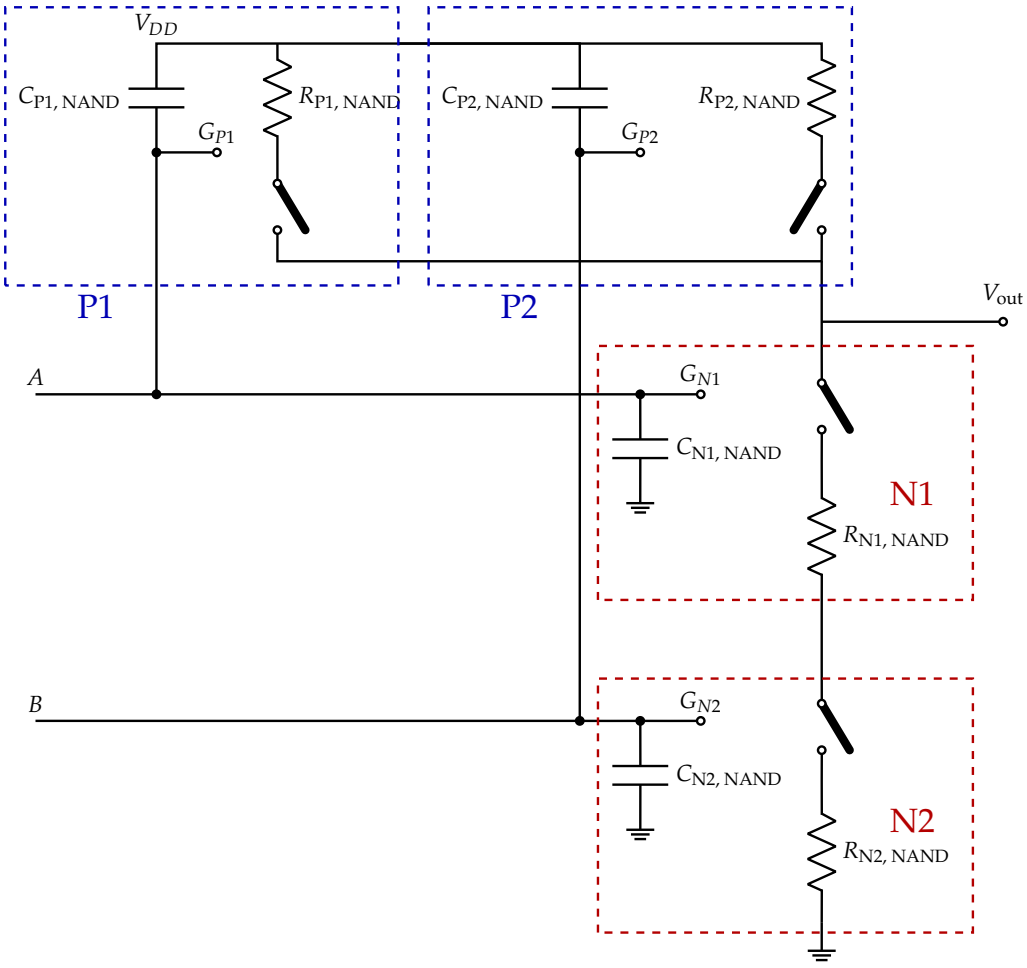


Figure 3: NAND Model: Capacitances

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