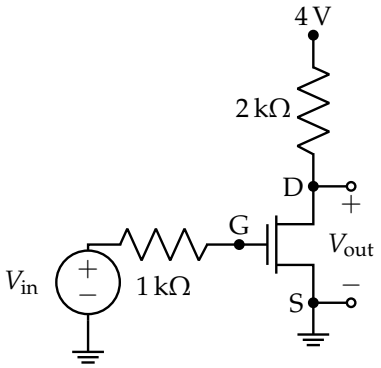
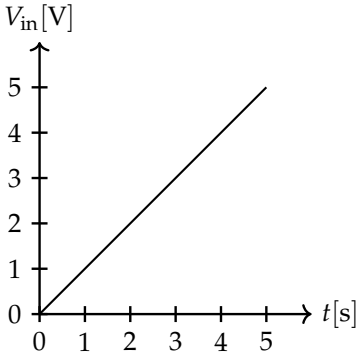
Discussion 2A

1. NMOS Logic Inverter

(a) We have an NMOS logic implementation of an inverter shown below. The circuit has a voltage input $V_{\text{in}}(t) = t$, $t \geq 0$, ($V_{\text{in}}(t) = 0\,\text{V}$ for $t \leq 0$) seen below.



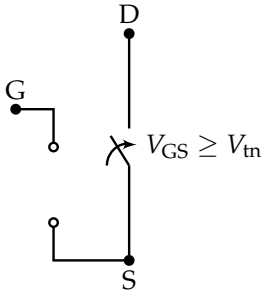
(a) NMOS Inverter



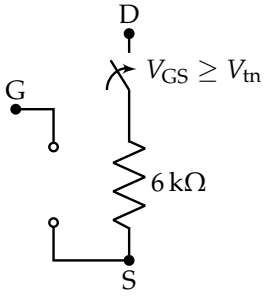
(b) Voltage input, V_{in}

Figure 1: Circuit figure and input signal.

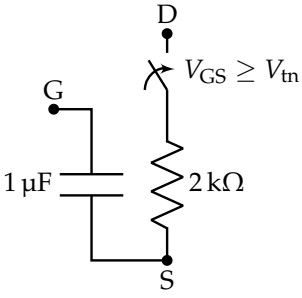
For the transistor models below, define the threshold voltage as $V_{\text{tn}} = 2\,\text{V}$. **Match each NMOS transistor model, plugged into the NMOS inverter circuit, with its corresponding V_{out} plot on the next page.** (Note: All capacitors are fully discharged at $t = 0$.)



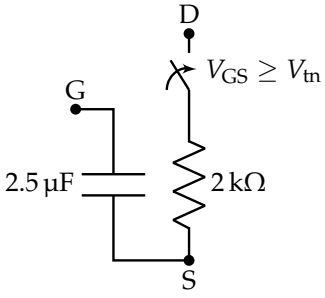
(I) Model I



(II) Model II

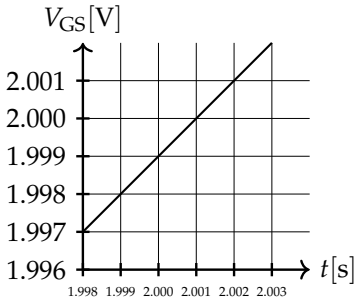


(III) Model III

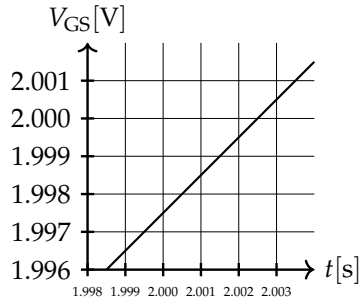


(IV) Model IV

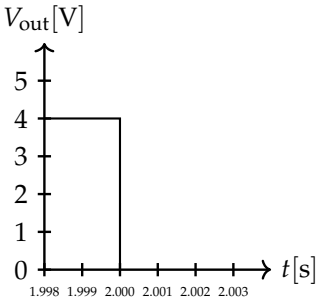
(HINT: You can use the below graphs to evaluate V_{GS} for Models III and IV. We recommend using a scratch page to draw out the NMOS Inverter circuit with the various transistor models plugged in.)



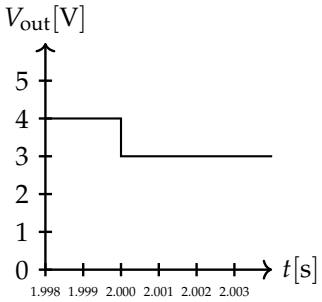
(a) V_{GS} for Model III



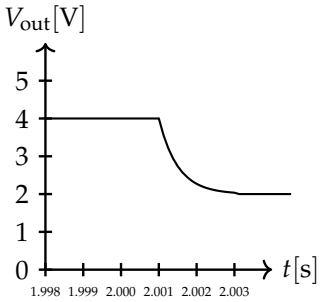
(b) V_{GS} for Model IV



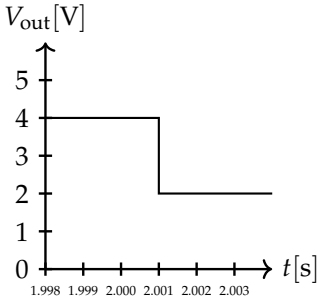
(A) Plot A



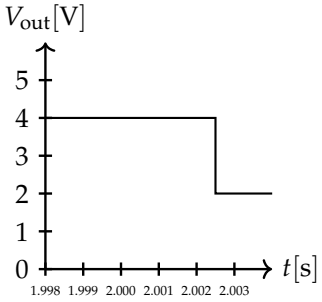
(B) Plot B



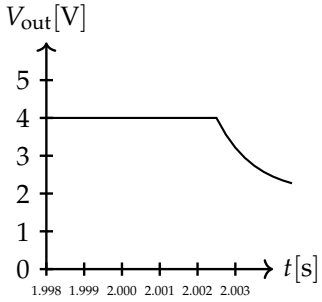
(C) Plot C



(D) Plot D



(E) Plot E

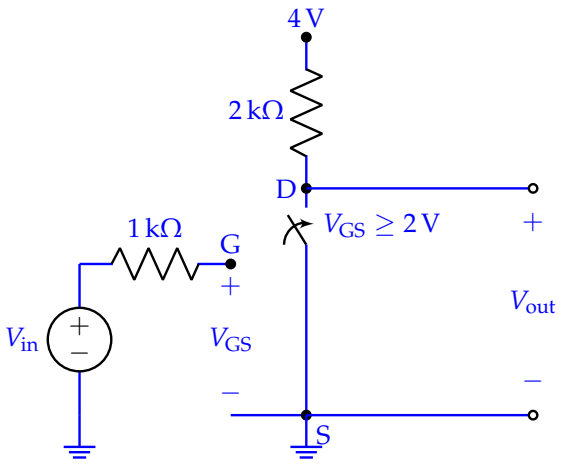


(F) Plot F

Model #	Plot A	Plot B	Plot C	Plot D	Plot E	Plot F
I	○	○	○	○	○	○
II	○	○	○	○	○	○
III	○	○	○	○	○	○
IV	○	○	○	○	○	○

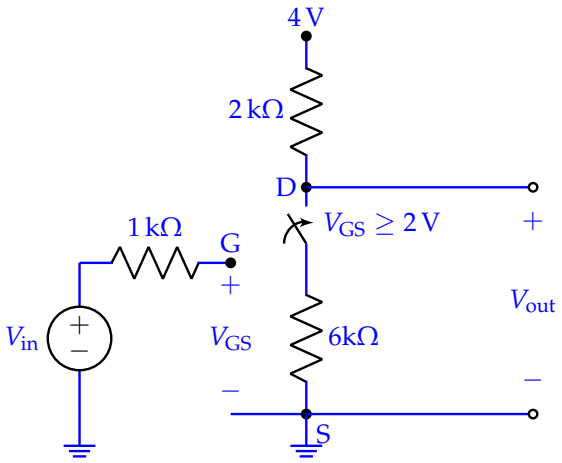
Solution: Let's analyze the four different models, case by case. We start with model I.

First, consider what V_{out} is when the switch is open. No current flows through the upper 2kΩ resistor as it is in series with an open switch. From Ohm's law we have that $\frac{V - V_{out}}{2k\Omega} = 0$, which implies that $V_{out} = 4V$ when the switch is open. By similar reasoning, the open over which V_{GS} is taken permits no current so $V_{GS} = V_{in}$. If this is the case, we see the transistor hit the threshold voltage, $V_{GS} = 2V$, when V_{in} does at $t = 2s$. So the switch turns on at $t = 2s$, and we should see the voltage on the output instantly drop to ground as there is a short from ground to V_{out}. The



plot that matches this behavior of switching from 4V to 0V at $t = 2$s is plot A.

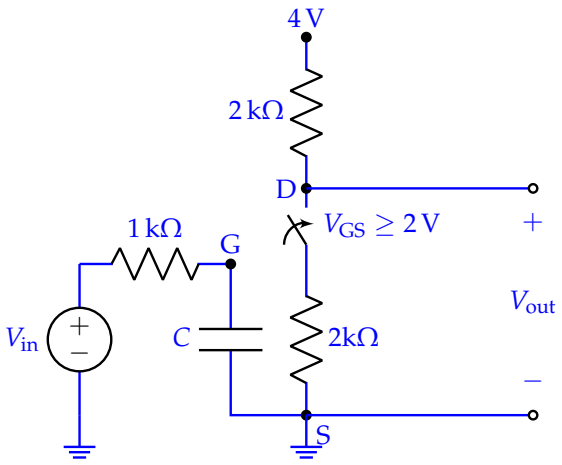
Let us examine model II. The circuit is depicted below. The only difference is that we now have a 6kΩ resistor from the drain to source, instead of a short of the previous model.



Given that this is the case, we should still see $V_{out} = 4$V at the beginning. V_{out} should then drop to some voltage at $t = 2$s. However, the voltage that it drops to is now determined by a voltage divider supplied by 4V, with 2kΩ and 6kΩ resistors in series, with the output V_{out} taken over the 6kΩ resistor. This means that $V_{out} = \frac{6\text{k}\Omega}{2\text{k}\Omega+6\text{k}\Omega} \cdot 4\text{V} = 3\text{V}$ for $t \geq 2$s when the switch closes. The plot that matches this behavior is plot B.

Consider now models III and IV, for which the only difference is the capacitance value. A circuit with the appropriate model drawn in is shown below.

Despite the addition of a capacitor, we still see the output is determined by a voltage divider without any capacitors as in the last case, so we should not see any charging or discharging behavior for V_{out}. This immediately rules out plots C and F, which have exponential decays to some steady state voltage. There is however, charging behavior for V_{GS}, but it is not necessary to solve the differential equation as the switch closure times are indicated by the hint plots as being $t = 2.001$s and $t = 2.0025$s for models III and IV respectively. Intuition regarding RC circuits is an alternative to the hint, as it is the case that it takes a longer time to charge up a larger capacitor, so there is a greater delay for the circuit with $C = 2.5\mu$F. Given that both models have the same



output resistor value in the voltage divider of 2kΩ, the output voltage should be $V_{out} = 2$V when the switch closes. Thus for model III, the correct plot is D, and for model IV the correct plot is E. All answers bubbled in are shown in a table below.

Model #	Plot A	Plot B	Plot C	Plot D	Plot E	Plot F
I	●	○	○	○	○	○
II	○	●	○	○	○	○
III	○	○	○	●	○	○
IV	○	○	○	○	●	○

2. An RC Circuit with a Dependent Source

Consider the following circuit ($V_{out}(0) = 0$):

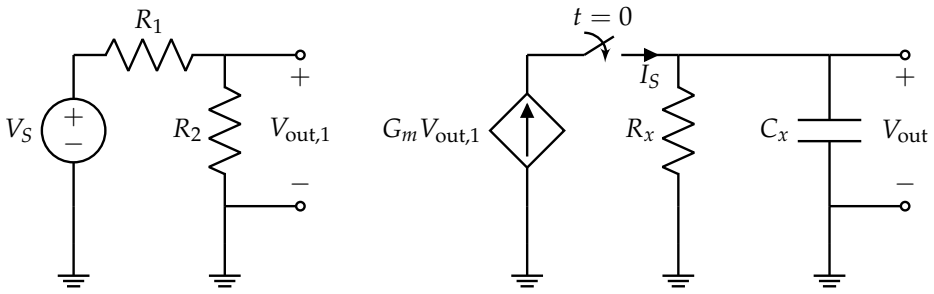


Figure 5

(a) **Find the differential equation for V_{out}.**

Solution: We first make note that we have a dependent source which is dependent on $V_{out,1}$. Thus we analyze the left circuit first.

We find $V_{out,1}$ by noting that the left circuit is a voltage divider. Thus,

$$V_{out,1} = \frac{R_2}{R_1 + R_2} V_S \tag{1}$$

Now, we begin our analysis on the right using KCL. I_S, I_R, and I_C are the dependent source, resistor, and capacitor currents respectively.

$$I_S = I_R + I_C \tag{2}$$

$$G_m V_{out,1} = \frac{V_{out}}{R_x} + C_x \frac{dV_{out}}{dt} \tag{3}$$

$$\frac{dV_{out}}{dt} + \frac{V_{out}}{R_x C_x} = \frac{G_m}{C_x} V_{out,1} \tag{4}$$

$$\frac{dV_{out}}{dt} + \frac{V_{out}}{R_x C_x} = \left(\frac{G_m}{C_x}\right)\left(\frac{R_2}{R_1 + R_2}\right) V_S \tag{5}$$

(b) **Find the time constant τ of the circuit.**

Solution: Looking at the differential equation which is now in our standard first-order form, we can see that the time constant is $\tau = \frac{1}{\frac{1}{R_x C_x}} = R_x C_x$, i.e. the reciprocal of the coefficient of V_{out}.

(c) **Draw a sketch of $V_{out}(t)$ for $t > 0$.** Make sure to include the initial value, asymptotic value, and the approximate value at the time constant (all in terms of the given variables). *(HINT: You can do this without solving the differential equation.)*

Solution: One way to plot the first order differential relationship would be to solve for V_{out} (using the solution form introduced in lecture and Discussion 01A). But we can also reason about the form of the solution as well.

First, we know what the shape of the graph looks like as it is the same as that of the charging RC described in the notes (increase with eventual tapering off to a steady state value).

Next, in order to find this steady state value for V_{out}, one has to consider what the circuit would look like in steady state. Capacitors can be represented as open circuits during steady state. Finally, we find the steady state value for V_{out} using Ohm's law.

$$V_{out} = I_S R_x \tag{6}$$

$$V_{out} = (G_m \frac{R_2}{R_1 + R_2} V_S)(R_x) \tag{7}$$

$$V_{out} = G_m R_x (\frac{R_2}{R_1 + R_2}) V_S \tag{8}$$

This gives:

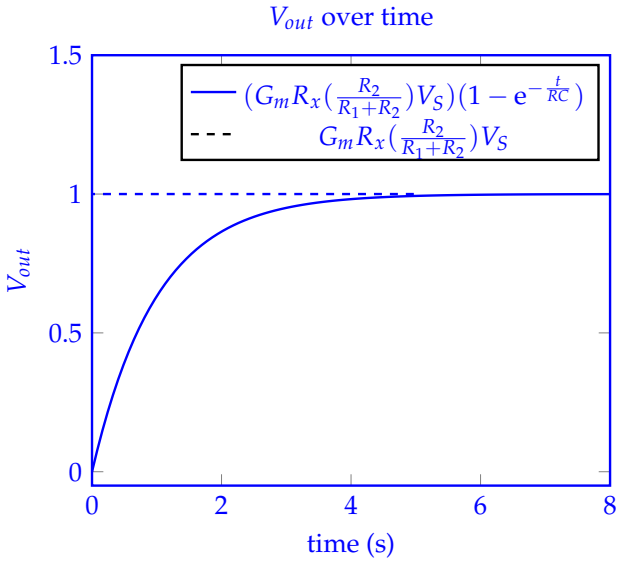


Figure 6

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